CR 72-588-030

Contract Number NA9-12110
DRL Line Item Number 34
DRD Number MA-129T

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TECHNICAL FINAL REPORT

Data Bus System Development Program

NOV. 1973

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS 77058

RCA CORPORATION
GOVERNMENT AND COMMERCIAL SYSTEMS
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ABSTRACT

This final report summarizes the results of the NASA Data Bus System Development Program performed under Contract NAS9-12110 by the RCA Corporation, Burlington, Mass.

The program involved the design, development and delivery of two different Data Bus Systems and the performance of seven different but related studies. Delivered items support the development by NASA of techniques for automated status monitoring, diagnostics, control and checkout of advanced spacecraft systems.

Both Data Bus Systems provide for the remote acquisition and distribution of data in excess of 20,000 messages per second at a clock rate of 5 megabits per second, with a probability of an undetected bit error of less than 1 bit in 10^{25}.

COS/MOS technology was utilized extensively to achieve low power consumption and high reliability, while maintaining compatibility with future LSI implementation.

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SUMMARY

Contract NAS 9-12110 and subsequent agreements constituted the defining work task instrument. The required Data Bus System development effort was specified in the contract as Exhibit "A" entitled "Statement of Work for Data Bus System Development" dated June 11, 1971. The effort was scheduled in accordance with Article 2 of the contract with subsequent agreements.

Two data bus systems were designed and fabricated, Data Bus System I (DBS-I) and Data Bus System II (DBS-II). The technical features of the delivered hardware include the following:

- 5 MHz Self-Clocking Data Bus
- Bi-Directional Communications Utilizing Manchester Code at Data Rates in Excess of 20,000 Words Per Second
- Utilization of MSI COS/MOS Technology
- Probability of Accepting an Erroneous Data Bit Less Than 1 in 10^{25}
- Low Power Consumption (50 to 1 Reduction in Quiescent Current Over P/MOS)
- Compatibility With Projected High Density Packaging (LSI)

Three distinct types of data bus remote terminals were developed, the Subsystem Interface Unit (SIU), the combination of an Electronic Interface Unit (EIU) and a Standard Interface Unit-Serial (SIU-S) and an SIU/Preprocessor (SIU-P).

The SIU designed for DBS-I provides the following capability:

Data Acquisition - Capable of acquiring both analog and digital data.

Analog

- Capable of sampling 32 analog data points.

- Analog data converted to binary code (8-bit) prior to transmission over data bus.
- Overvoltage protection provided.

Digital

- Capable of sampling 64 digital data points in 8-bit bytes.
- Compatible with TTL Logic.
- Overvoltage protection provided.

Data Distribution - Capable of outputting both analog and digital data

Analog

- Capable of outputting two analog signals to user subsystem as instructed by coded message.
- Short circuit protection provided.

Digital

- Capable of outputting 64 digital data signals in 8-bit bytes
- Compatible with TTL Logic.
- Over and under voltage protected.

Self-Test - Provides self-check capability and status reporting via bus messages.

The Electronic Interface Units (EIU) provide the following functions:

Data Acquisition - Capable of acquiring both analog and digital data.

Analog

- Capable of sampling 32 analog data points
- Analog data converted to binary code prior to transmission over data bus.
- Overvoltage protection provided

Digital

- Capable of sampling 256 digital data points in 8-bit bytes.

- Compatible with TTL Logic.
- Overvoltage protection provided.

Data Distribution - Capable of outputting both analog and digital data.

Analog

- Capable of outputting eight analog signals to user subsystem as instructed by coded message.
- Short circuit protection provided.

Digital

- Capable of outputting 64 digital data bits in 8-bit bytes.
- Compatible with TTL logic
- Over and under voltage protection

Self-Test - Provides self-check capability and status reporting via bus messages.

The Standard Interface Units (SIU-S) provide the following capabilities:

- Data Bus interface for 5 MHz operation
- Isolated transmit ports for EIU interface.
- Isolated receive ports for EIU interface.

The SIU/Preprocessor provides the identical functions as the SIU and in addition includes the preprocessor interface required for accessing the subsystem for data acquisition and distribution. The additional SIU-P capability includes the following:

- Subsystem interface for data acquisition and distribution to the computer for local program operation.
- Non-interrupt interrogation of SIU-P operational mode and status.
- Commands via the data bus to halt, interrupt, continue, or start the commanded local processor programs.

The Bus Control Unit (BCU) was developed for DBS-II. The BCU provides the following capabilities.

- Generation of four isolated and synchronized time-slots to the four computers (16 ports).
- Four manually selected time-slot sequences.
- Interface to the four data bus cables.
- Four isolated transmit interfaces to the four computers (16 ports).
- Four isolated receiver interfaces to the four computers (16 ports).

A Bus Exerciser was developed for each system to simulate the DMS computers for checkout and evaluation of the Data Bus System. The Bus Exerciser is capable of operating DBS-I, including all the operational and display functions. In addition to these functions, the following capabilities have been added for DBS-II operation:

- Simulation of DMS computer interface for operation of DBS-II with BCUs.
- Vote logic for time slot error detection of BCUs.

The Bus Exerciser control and display panel provides the following functions for the demonstration of the operational capabilities of the Data Bus Systems:

- Transmits instructions and data to any of 128 remote terminals.
- Accepts and displays the remote terminals response data.
- Operates the data bus in both simplex and quad-redundant modes of operation.
- Redundant operation on returned data from remote terminals may be accepted, composed, and displayed - the display indicates the extent to which the four return messages agree or disagree.
- Utilizes full-scale mini-computer (NOVA 1200) to simulate operational modes and cyclic error control generation.

The major components of DBS-I are one Bus Exerciser, four twisted shield-pair cable sets, 16 SIU's and eight SIU-P's. The major components of DBS-II are one Bus Exerciser, four twisted shield-pair cable sets, 12 SIU-S's, four BCU's and eight EIU's.

Seven studies complete the work tasks required. They are:

Bus Control Unit Requirements Study

- Requirements Analysis
  - Four Central Computers
  - Four Bus Control Units
- Task Allocation (BCU Versus Central Computer)
- Cross-Strapping
- Self-Test Features
- Diagnosis, Fault Isolation, and Redundancy Switching
- Bus System Management
- Data Validation
- Command Verification
- Accommodation of Down Link Requirements
- Preliminary BCU Design

Subsystem Interface Unit/Preprocessor Interface Study

- Computer/Bus Interface
- Computer/Subsystem Interface (Acquisition and Distribution)
- Priority Assignment
- Lockout Capability
  1) Computer Time - Critical Routines
  2) Computer Malfunction
  3) DMS Test Point Access
- Recommended Design of SIU-P

Data Bus System/Vehicle Subsystem Interface-Redundancy Interface Analysis

- Interface with subsystem of fewer levels than FO-FO-FS bus
- Impact on data bus reliability and redundancy
- Design to minimize impact of recommended interfaces.

SIU/Vehicle Subsystem Interface-Logic Level Analysis

- Optimum Logic Levels
- Required Noise Margin
- Noise Rejection Requirements
- Special Designs

Integrated Diagnostics Performance Analysis

Based on "An Engineering Study on Onboard Checkout Techniques" (NAS 9-11139)

- Allocation of Onboard Checkout Functions
- Comparative Evaluation with SIU Design
- Standardization of SIU/Subsystem I/O Modules
- Ease of Maintenance
- Minimization of Spares
- Self-Test and Checkout
- Design for MSI and LSI
- Required Data Acquisition and Processing Times

Self-Powered Data Bus

- Techniques for Routing Terminal Power via the Data Bus
- Recommended Power Routing Technique
- Identification of Technique Impact on Data Bus System
- Transceiver Design
- Breadboard of Technique

Comparison with ARINC Standard Interface

- Design Comparison with ARINC Char. 575
- Major Differences
- Required Changes for Compatibility

CONCLUSIONS

The data items as defined in NASA MSC contract NAS9-12110 to RCA Corporation dated June 30, 1971 have been completed and delivered to NASA. The data items have been accepted by NASA and are in full compliance with all contractual specifications and agreements. Integration of delivered hardware within the Space Shuttle Mock-up is proceeding under NASA supervision and control.

The hardware delivered provides an operational breadboard which may be readily altered as the shuttle subsystems vary in type and/or quantity or as system concepts are modified. The hardware thus provides the vehicle for the implementation and evaluation of a data bus in the Space Shuttle. The hardware development resulted in the practical implementation of design concepts providing a system operation capability which enhances data bus utilization in advanced systems.

The major design areas enhanced by this hardware development include the following:

- Reliable multi-port data transfer at a 5 MHz rate on a twisted shield pair.
- Utilization of cyclic error codes to reduce probability of an undetected erroneous bit to less than 1 bit in 10^{25}.
- Practical implementation of COS/MOS circuits for critical low power applications.
- Self-clocking decoding techniques which provide long distance, high data rate transfer capability.

RECOMMENDATIONS

The development of the Data Bus Systems and their successful performance logically leads to further refinement. The areas for further development include both hardware and design aspects and are as follows:

- Fabrication of a prototype unit utilizing COS/MOS LSI and hybrids.
- Investigation of alternate message preamble and decoding techniques to increase cable transmission distances.
- Evaluation of required type and mix of subsystem interface signals encountered in the projected advanced space vehicles (shuttle, station, etc.) for optimum module commonality.
- Design, fabrication and test of an SIU-P interface for one of the potential space applicable preprocessors (SUMC, CDC 469, etc.)

DETAILED DESCRIPTION

Current Space Station and Space Shuttle study efforts have developed Data Management System (DMS) concepts which utilize a Data Bus System to acquire and distribute data and commands to and from vehicle subsystems to substantially reduce vehicle wiring. The bus itself is a twisted-shielded pair cable and utilizes time division multiplexing and pulse code modulation techniques to serially transfer data and commands between the DMS computer or computers and the vehicle subsystems. The Data Bus Design was required to supply communications over 500 feet of cable loaded with up to 128 remote terminals. The test configuration of the data bus, shown in Figure 1, provides for 20 SIU tie-junctions with two data bus branch points for DBS-I. The data bus configuration for DBS-II is identical where SIU-S's and EIU's are used instead of SIU's. Transformer coupling was used to provide dc isolation and common mode rejection. Error control was accomplished by using a 15 bit cyclic error code which provided the probability of an undetected bit error of 10^{-25} with a bus error rate (bit and burst errors due to noise) of 10^{-6}.

Two Data Bus Systems were designed and fabricated in accordance with the NASA Statement of Work for Data Bus System Development dated June 11, 1971. The subsystem configuration for DBS-I and DBS-II provides the development hardware necessary to evaluate two competitive redundant philosophies. The major components of DBS-I are one Bus Exerciser, four twisted-shielded pair cable sets (490 foot overall length - see Table 1), 16 SIU's and 8 SIU-P's. DBS-II consists of one Bus Exerciser, four Data Bus Cable Sets the same as DBS-I, 12 SIU-S's, four BCU's and eight EIU's.

The Bus Exerciser contains a high-speed minicomputer, control and display panels, teletype-writer, and a data bus buffer and control unit. The computer is used to perform voting on data bus messages, detect errors received from the SIU's, generate errors for checking out the SIU's and compare received test data values with prestored limits. The data bus buffer and control unit acts as an interface between the computer and data bus. This unit interfaces with the computer direct memory access channel and converts the parallel computer words into serial format suitable for the quad redundant data bus operation. The unit also performs the reverse operation by receiving serial inputs from the SIU's and converting them to parallel

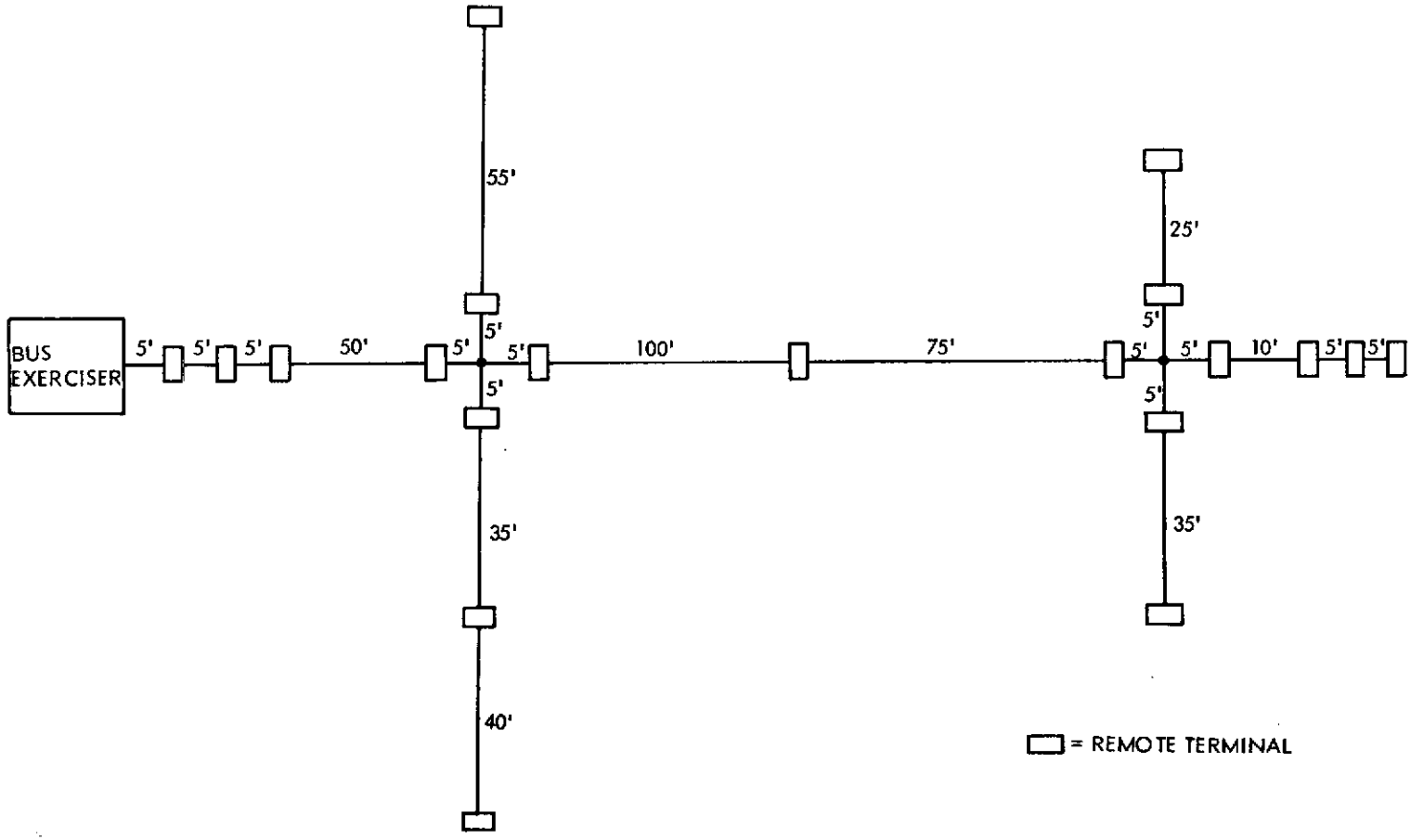

Figure 1. Data Bus Configuration

Table 1. Data Buses, Quantity and Length

Length (Feet)	Data Bus 1, 2, 3	Data Bus 4
5	13 Ea	3
10	1 Ea	-
25	1 Ea	1
30	-	1
35	2 Ea	-
40	1 Ea	1
50	1 Ea	-
55	1 Ea	-
60	-	2
75	1 Ea	-
80	-	1
100	1 Ea	-
180	-	1

words for the computer. See Figure 2 for display and control functions provided on the Bus Exerciser panel.

Each data bus is a twisted shielded pair cable. The data bus is terminated in its characteristic impedance at each of the tie junctions for the SIU's such that there are no signal reflections. The bus has a bandwidth of approximately 15 MHz so that a 5 megabit/second data train can be transmitted up to 500 feet with acceptable signal degradation on a twisted shielded pair. The serial data train transferred to and from the Bus Exerciser and the SIU's is a Manchester coded biphase self-clocking signal.

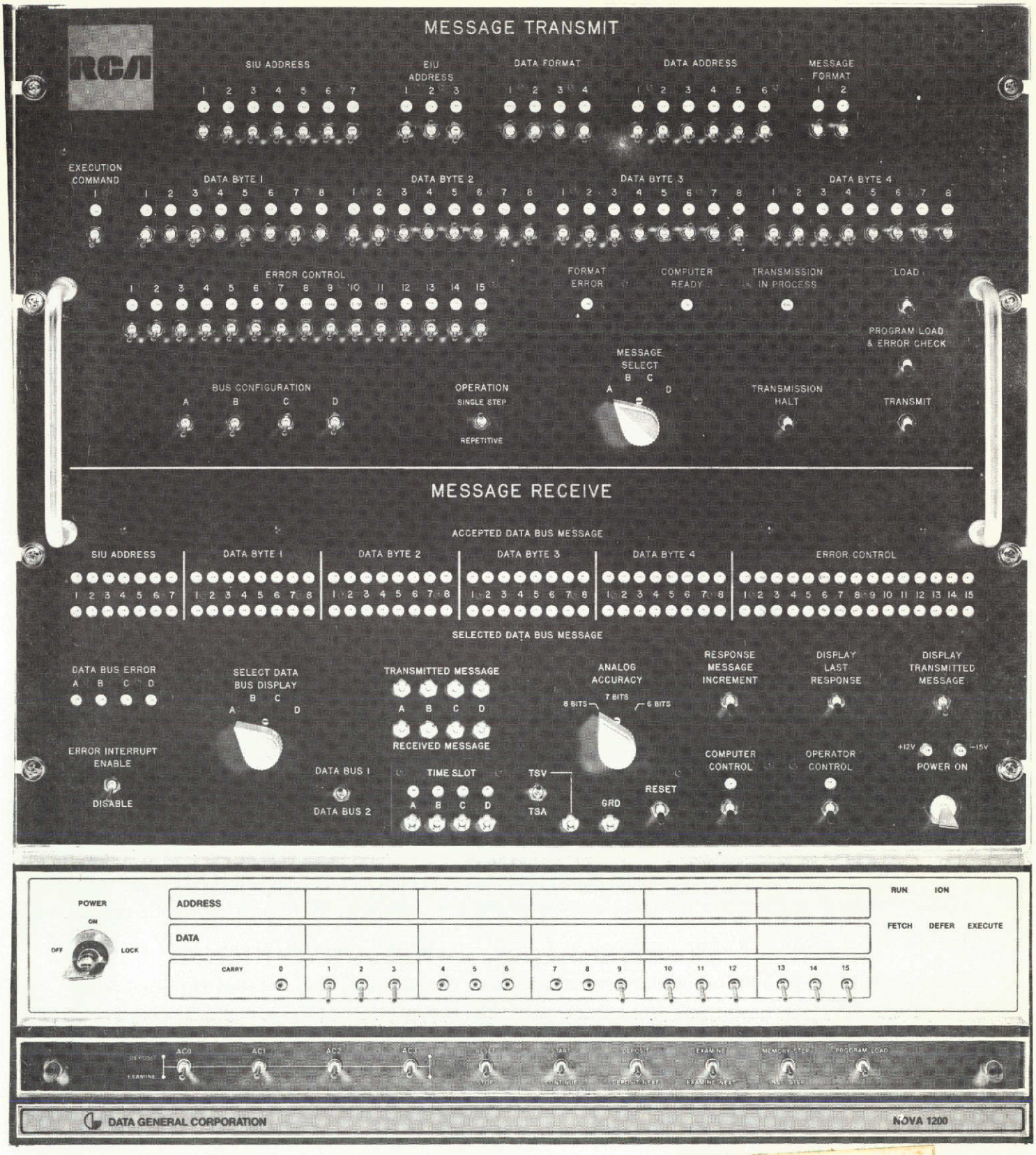

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Figure 2. Bus Exerciser

Data Bus System I

DBS-I (shown in Figure 3) is a quad-redundant data acquisition, storage and subsystem control interface between the space shuttle central computer and associated on-board subsystems. The system provides FO-FO-FS operation where the quad-redundant systems are maintained in an active state during critical mission phases. Figure 4 shows the quad redundant subsystem interconnectivity for DBS-I.

The two types of remote terminals developed for DBS-I, the SIU and the SIU-P, both perform the complete integrated function between the data bus and the user subsystem. They also provide self-test and status reporting. Their major functions are split into three sections: Data Bus Interface, Sequence Control, and Subsystem Interface. The SIU is shown in Figure 5 and a simplified block diagram of the unit is shown in Figure 6.

Data Bus System II

DBS-II (shown in Figure 7) provides passive redundancy, that is, only one section is actively energized until a failure occurs within the string and then an alternate operational interconnectivity path is energized. Figure 8 shows the quad redundant interconnectivity. DBS-II includes a quad redundant Bus Control Unit (BCU) which provides the interface between the data bus and four dedicated computers. The design is such that,after any three failures, the system is still operational. Figure 9 shows the BCU/computer interconnectivity.

Figure 10 is a simplified block diagram DBS-II. The BCU is designed to provide bus access to as many as four computers as indicated, however the Bus Exerciser is required to exercise only one bus at a time. The remote terminals which connect the busses to the redundant subsystem are physically divided into two sections, the transceiver and the input/output section. The transceiver section that provides serial interface with the data bus is referred to as the SIU-S. The input/output section is referred to as the EIU. Each EIU has four input/output busses to connect to four SIU-S's, and each SIU-S is capable of connecting up to eight EIU's to the data bus.

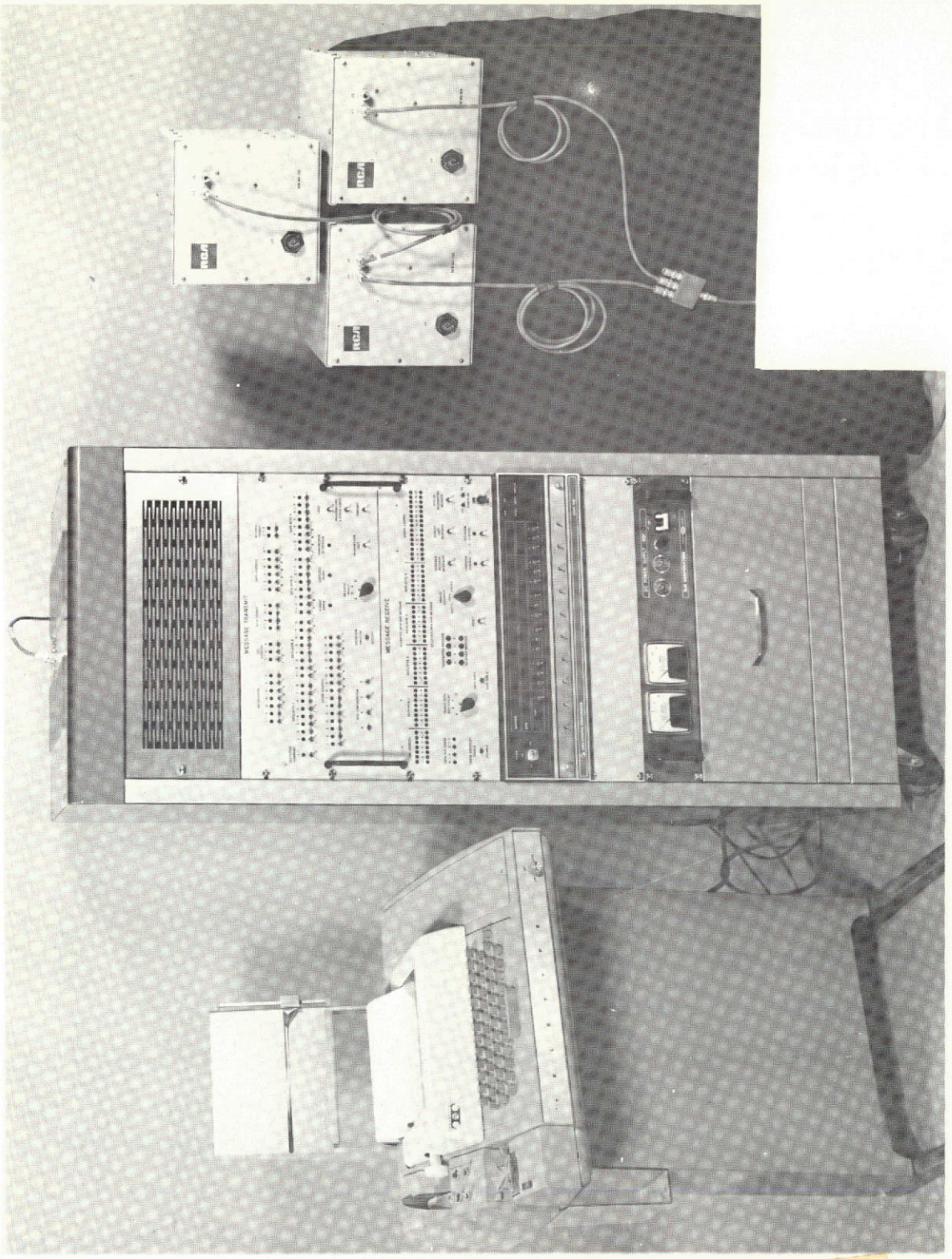

Figure 3. Components of Data Bus System I

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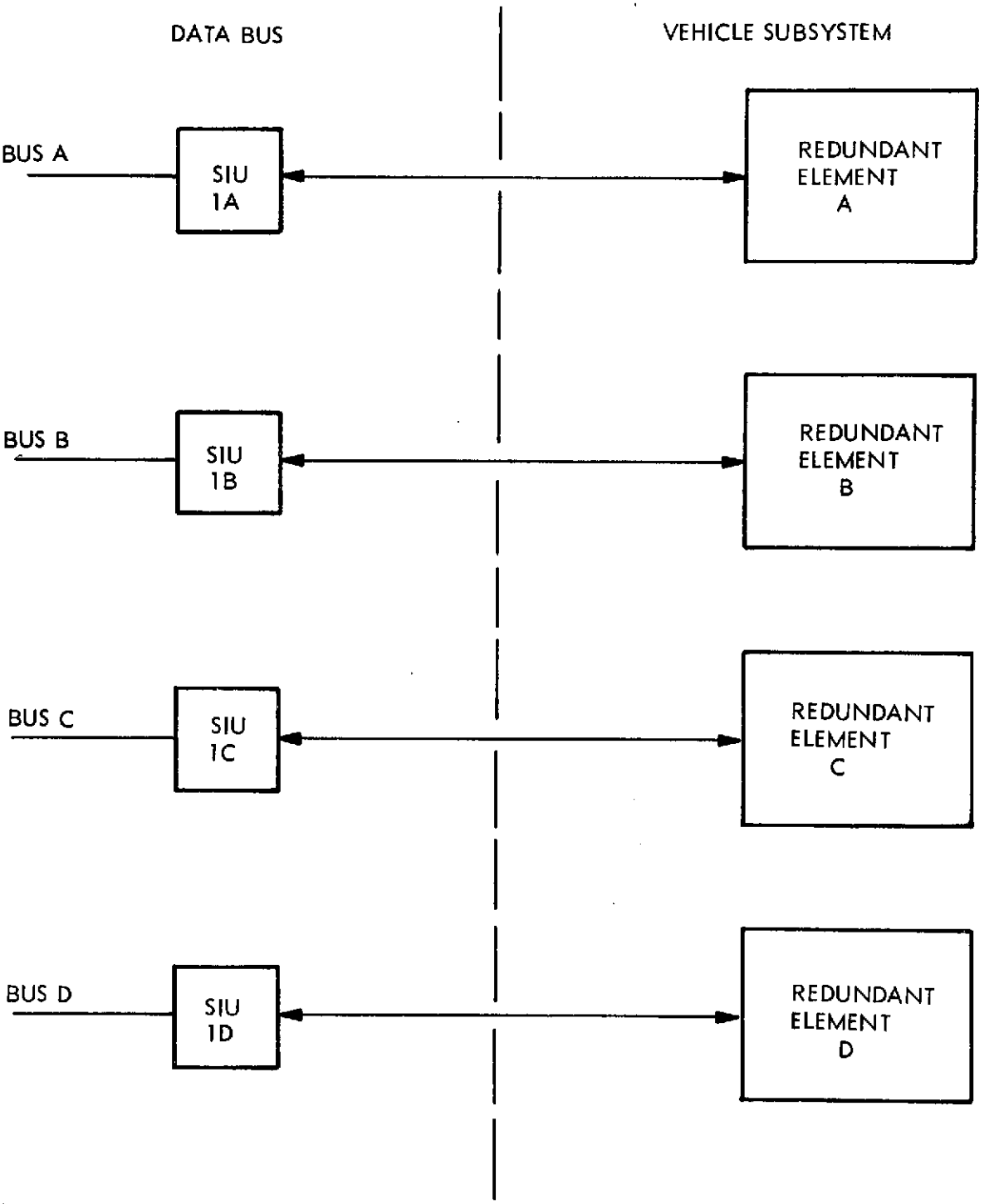


Figure 4. Subsystem Interconnectivity Bus System I

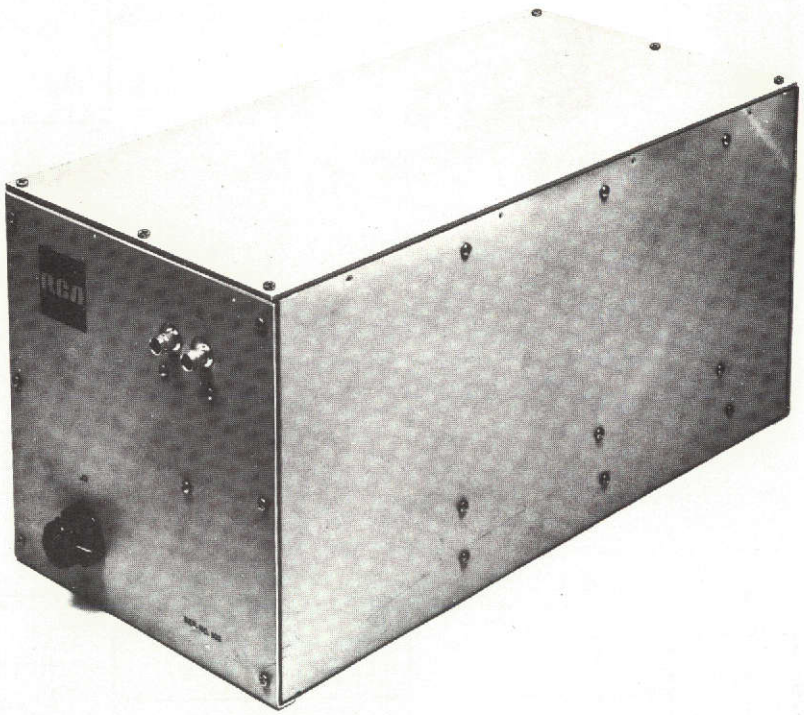
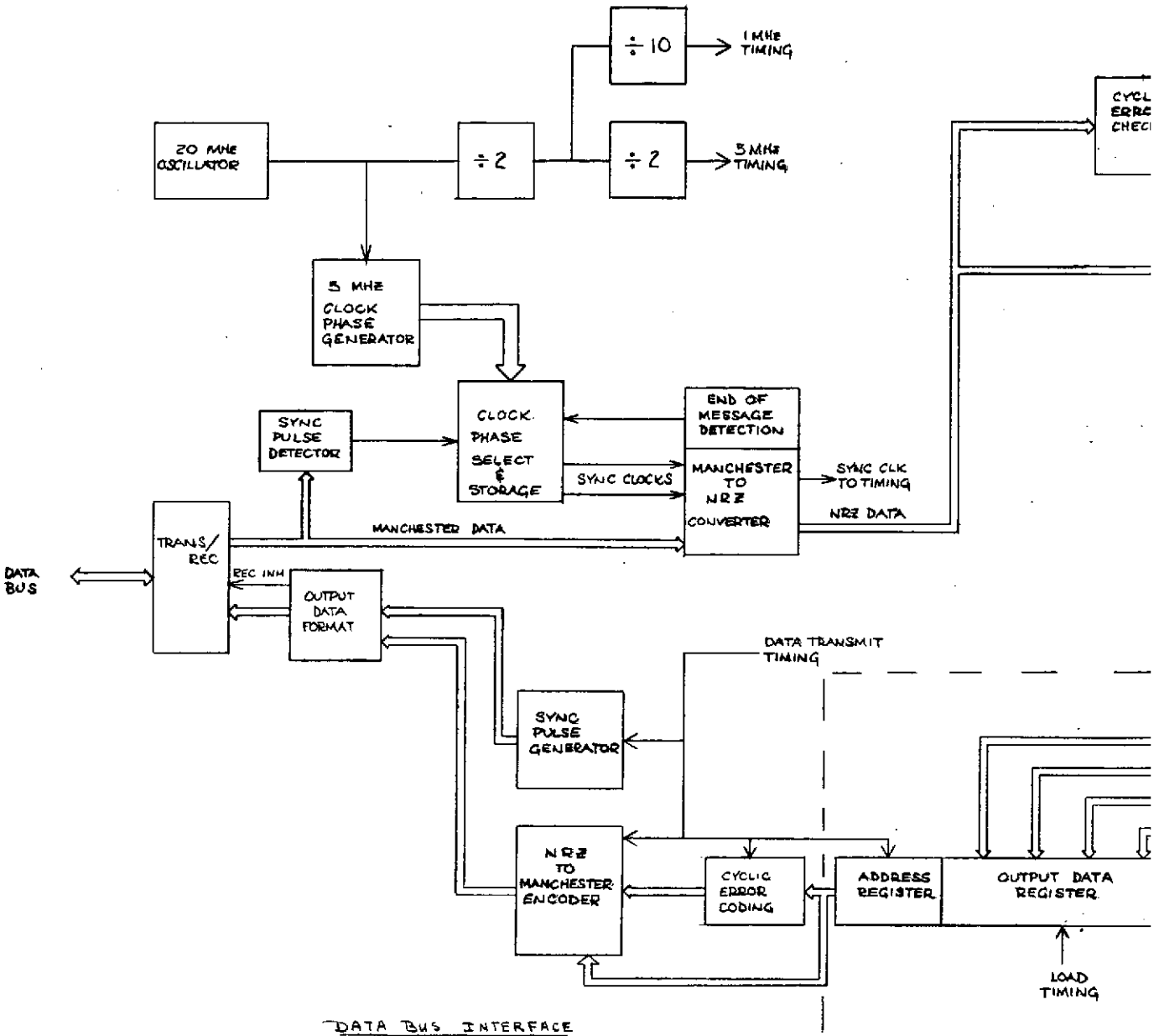
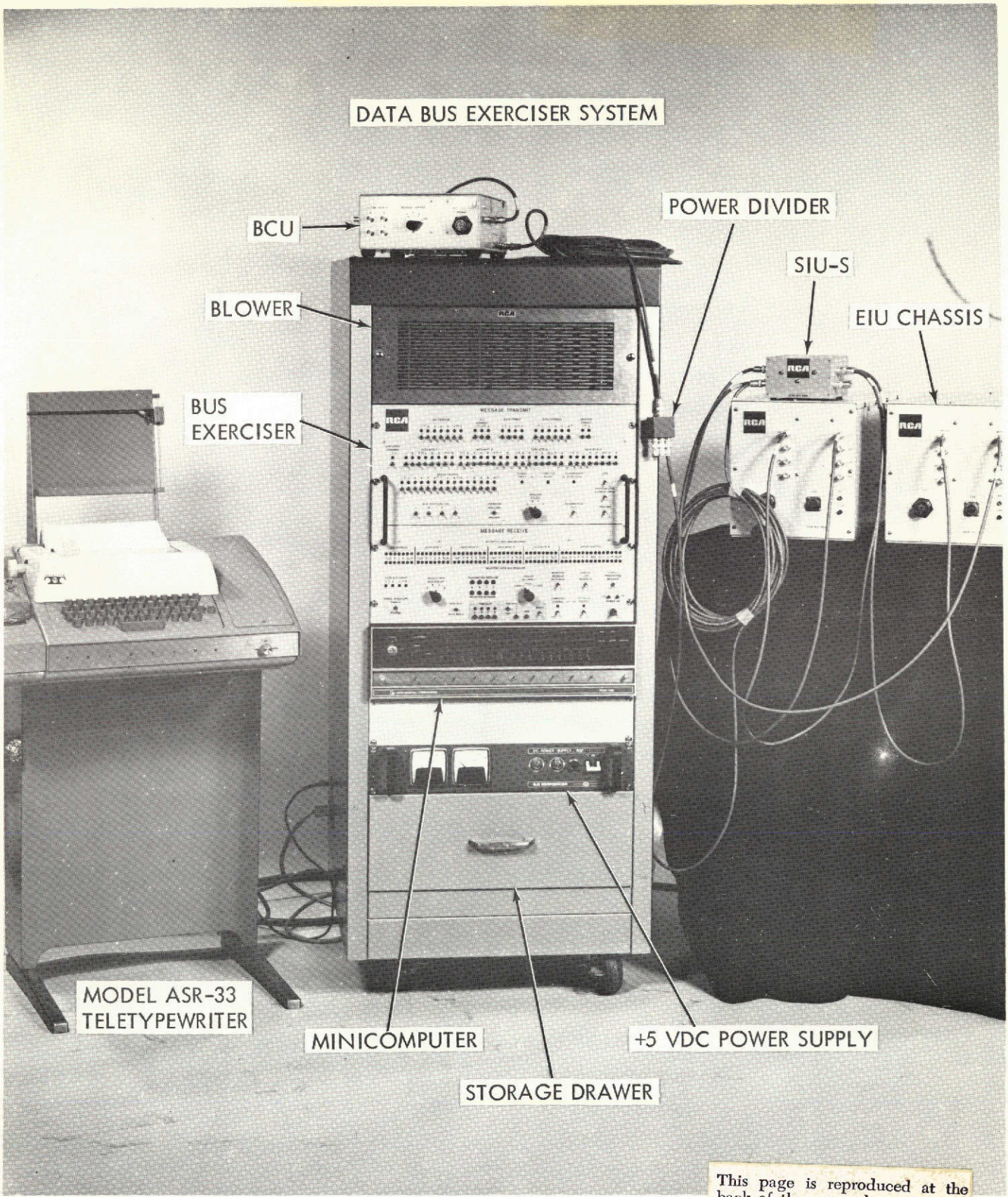


Figure 5. Subsystem Interface Unit (SIU)


÷ 10
1 MHz TIMING
20 MHz OSCILLATOR
÷ 2
÷ 2
5 MHz TIMING
5 MHz CLOCK PHASE GENERATOR
SYNC PULSE DETECTOR
CLOCK PHASE SELECT & STORAGE
END OF MESSAGE DETECTION
MANCHESTER TO NRZ CONVERTER
SYNC CLK TO TIMING
NRZ DATA
SYNC CLOCKS
MANCHESTER DATA
TRANS/ REC
DATA BUS
REC INH
OUTPUT DATA FORMAT
DATA TRANSMIT TIMING
SYNC PULSE GENERATOR
NRZ TO MANCHESTER ENCODER
CYCLIC ERROR CODING
ADDRESS REGISTER
OUTPUT DATA REGISTER
LOAD TIMING
DATA BUS INTERFACE
SEQUENCE

FOLDOUT FRAME 2



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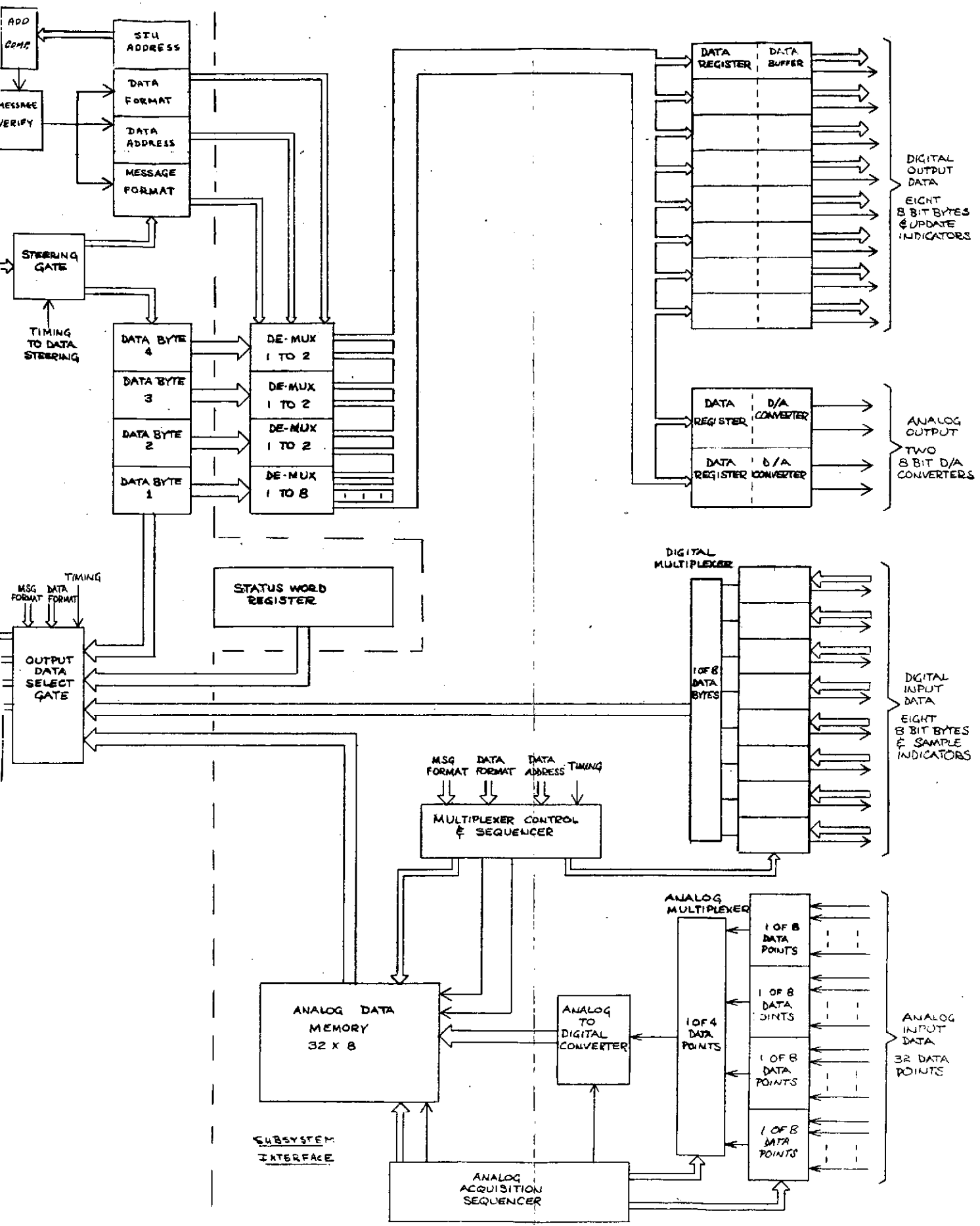
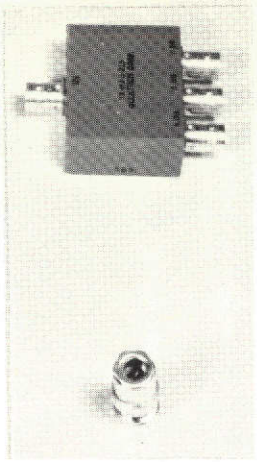


Figure 6. Simplified Block Diagram of SIU

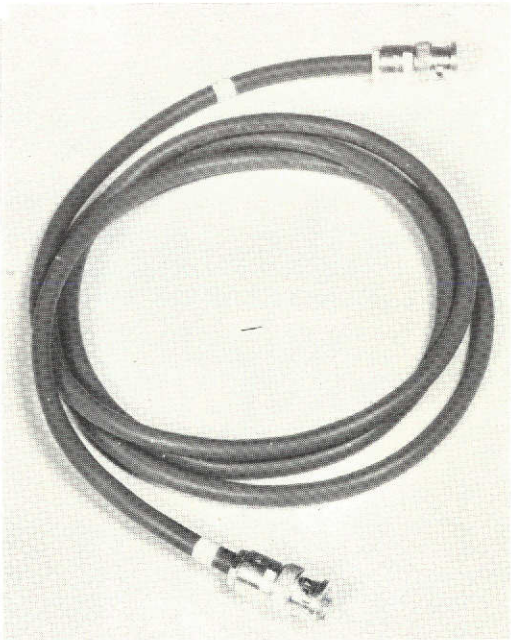
FOLDOUT FRAME



POWER DIVIDERS
(2 PER DATA BUS)
OLEKTRON CORP.
MODEL TX-HJ-3-215

LINE TERMINATIONS
(AMPHENOL 31-224
CONNECTOR WITH
RN60C75ROF RESISTOR)

DATA BUS
490-FOOT (MULTISECTIONED)
TROMPETER
ELECTRONICS
TWINAX CABLE
TWC-78-2



AMPHENOL
31-224
CONNECTORS

Figure 7. Components of Data Bus System II

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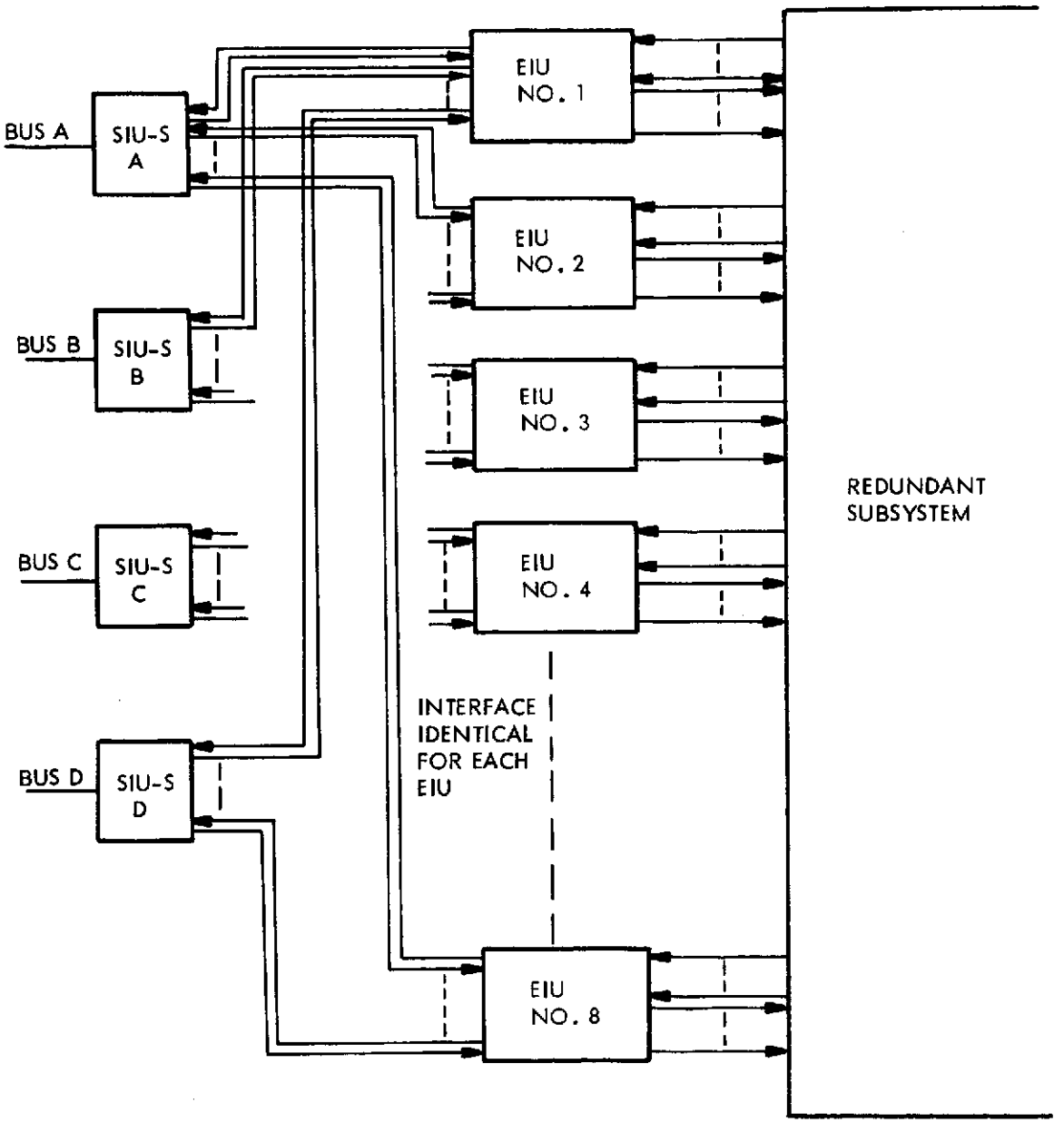


Figure 8. Subsystem Interconnectivity Bus System II

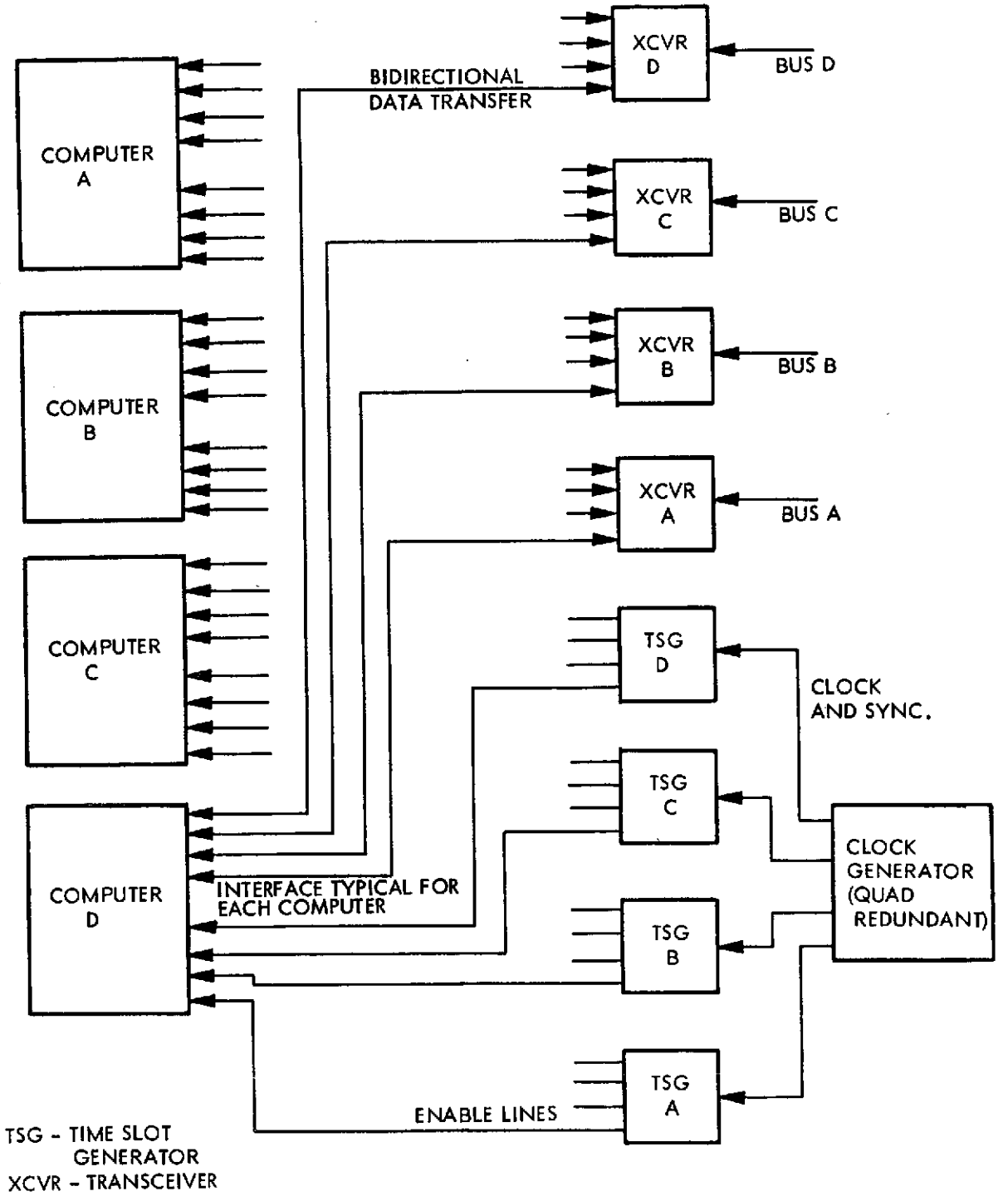


Figure 9. BCU/Computer Interconnectivity Bus System II

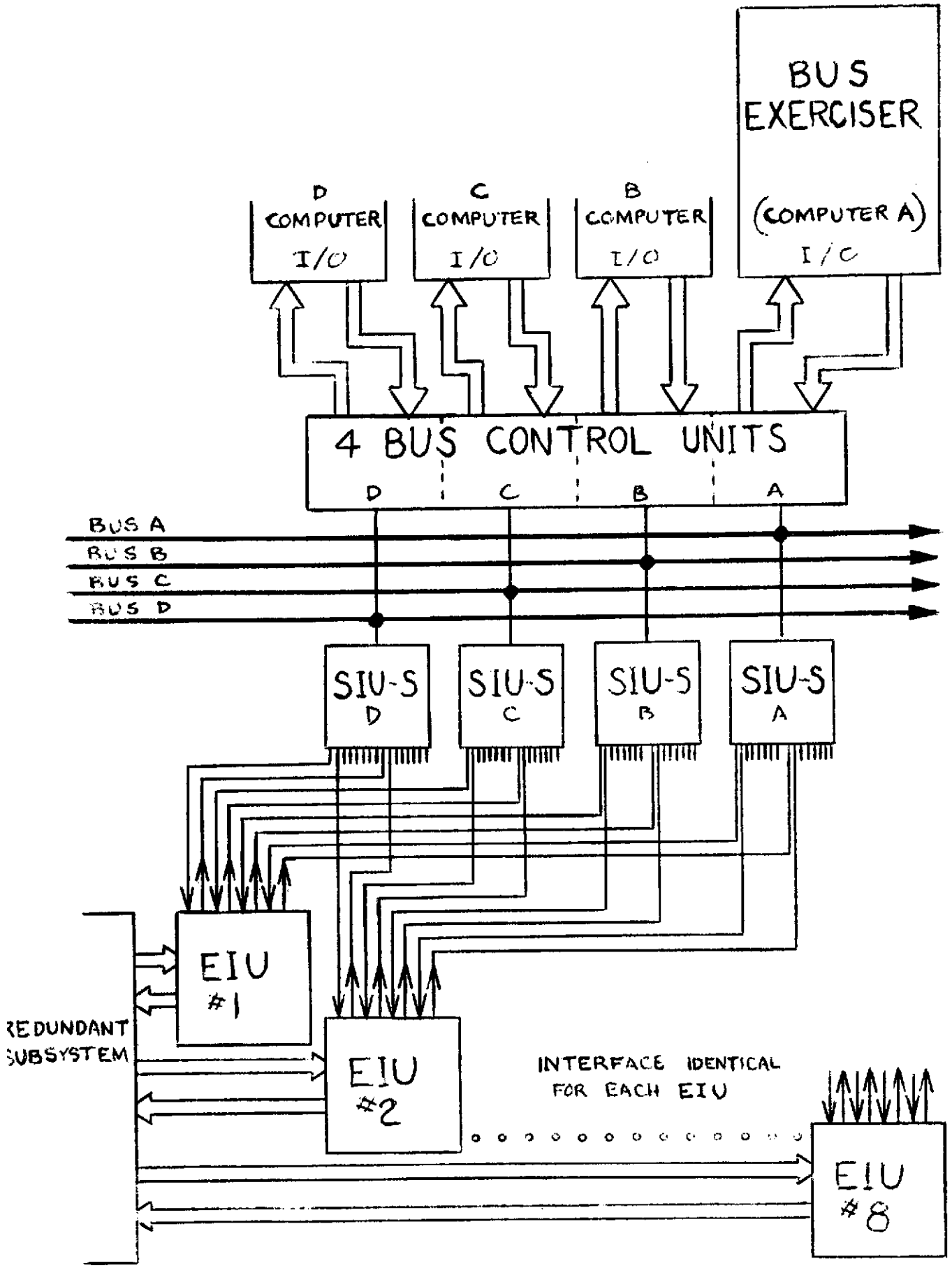


Figure 10. Simplified Block Diagram of Data Bus System II

Figure 11 is a simplified block diagram of the EIU for DBS-II. The major functions are: Data Bus Interface (DBI); Sequence Control (SC); and Subsystem Interface (SSI).

The purpose of the SIU-S is to provide an interface between the Data Bus and the various EIUs. The SIU-S becomes a message repeater and distributor for each group of redundant subsystems interconnected to the Data Bus with an EIU.

Message Structures

Data bus message formats have been configured to permit the sampling of analog data (8-bit) at a rate of 20,000 samples per second. This has resulted in the selection of a 5 megabit/second data transfer rate and a variable message format which allows for short (3 byte) format for data requests and address (message) verification. Command messages are 4 bytes, while data responses are 5 bytes. Transmission to and from the preprocessor may be accomplished by message formats up to 128 bytes in length.

The message formats provide the following message capability:

Acquisition (Analog and Digital)

Single Byte	(8 bits)
Block	(4-8 bit bytes)
All	(all data in successive block message)

Distribution (Analog and Digital)

Single Byte	(8 bits)
Block	(4-8 bit bytes)
All	(Clearing all data to zero)

In addition to this capability, the SIU-P provides for the acquisition and update message format of two bytes for computer I/O compatibility.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

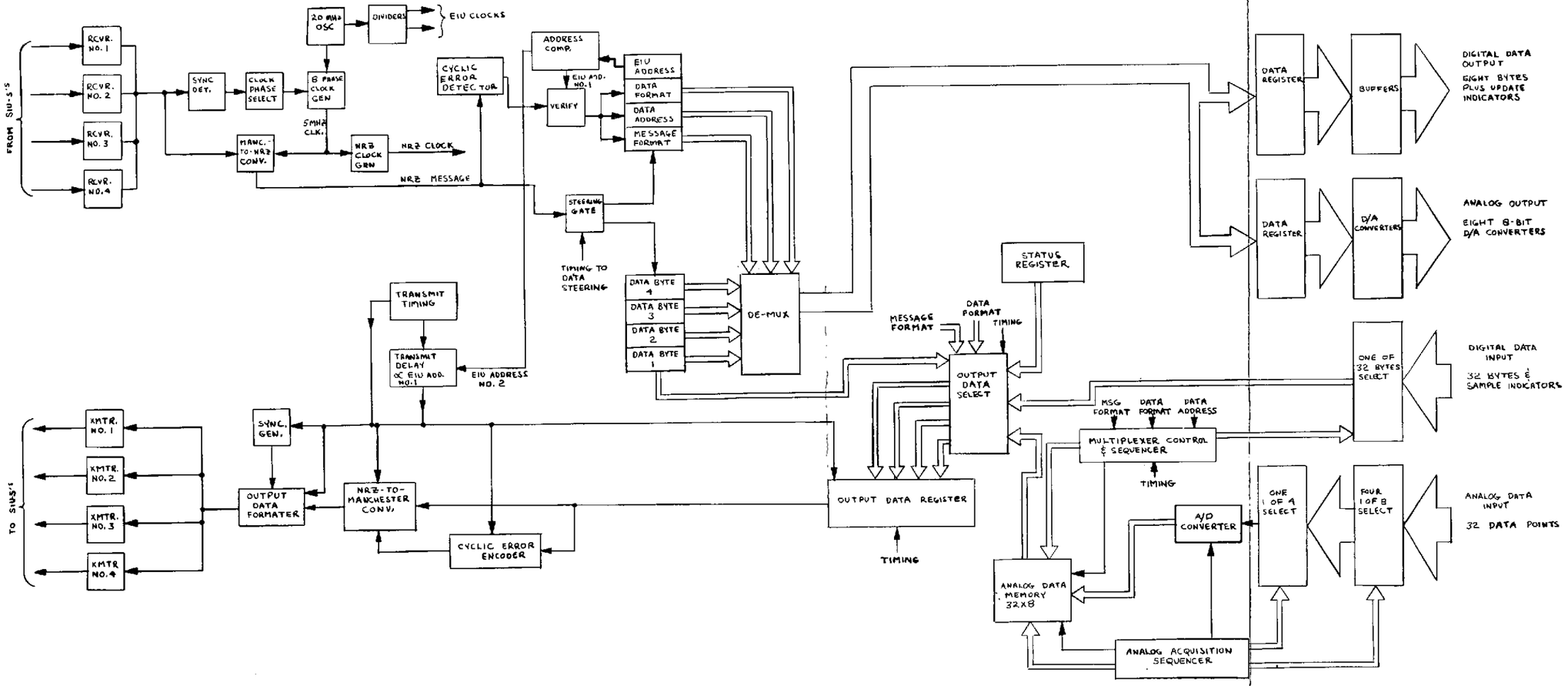


Figure 11. Simplified Block Diagram of EIU

The message rate provides for the updating or acquisition (command and response) of a single byte in excess of 18,000 times per second.

The subsystem data points for both Bus Systems I and II impose the same electrical requirements but the number of data points differ. Table 2 itemizes the acquisition and distribution data points for the two data bus systems.

Table 2. Acquisition and Distribution Data Points

	Data Points	
Acquisition	DBS-I	DBS-II
Analog	32	32
Digital	64	256
Distribution		
Analog	2	8
Digital	64	64

The acquisition data point characteristics for the data bus systems are as follows:

Analog

Signal Range:	0 to +5 Volts
Signal Source Impedance	5000 ohms maximum
Input Impedance:	
During Sampling:	1 megohm minimum
During Non-Sampling and Power Off:	10 megohm minimum
Overvoltage Protection:	+32 Volts to -2 Volts
Conversion Resolution:	8 bits
Conversion Accuracy:	0.5%

Digital

Signal Source:	TTL compatible
Sample Gate/8 bits:	Logic "1" encompassing sample period
Overvoltage Protection:	+32 Volts to -2 Volts

The distribution data point characteristics for the data bus systems are as follows:

Analog

Signal Range:	0 to +5 Volts
Signal Source Impedance:	100 ohms maximum
Load Impedance:	50K ohms minimum
Overvoltage Protection:	+32 Volts to 0 Volts (GND)
Voltage Increments:	20 Millivolts
Voltage Accuracy:	1.0%

Digital

Signal Outputs:	TTL compatible
Signal Gate/8 bits:	1 microsecond pulse spanning update
Overvoltage Protection:	+32 volts to 0 volts (GND)

The message structures for DBS-I are essentially the same as those shown in Figure 12 except for the response message containing no EIU address.

A data acquisition command message will result in a data response message, containing the requested data. A data update command message will result in a verify response, indicating that the addressed EIU has received and acknowledged the update command. The functions of the various segments of the message are detailed in the subsequent paragraphs.

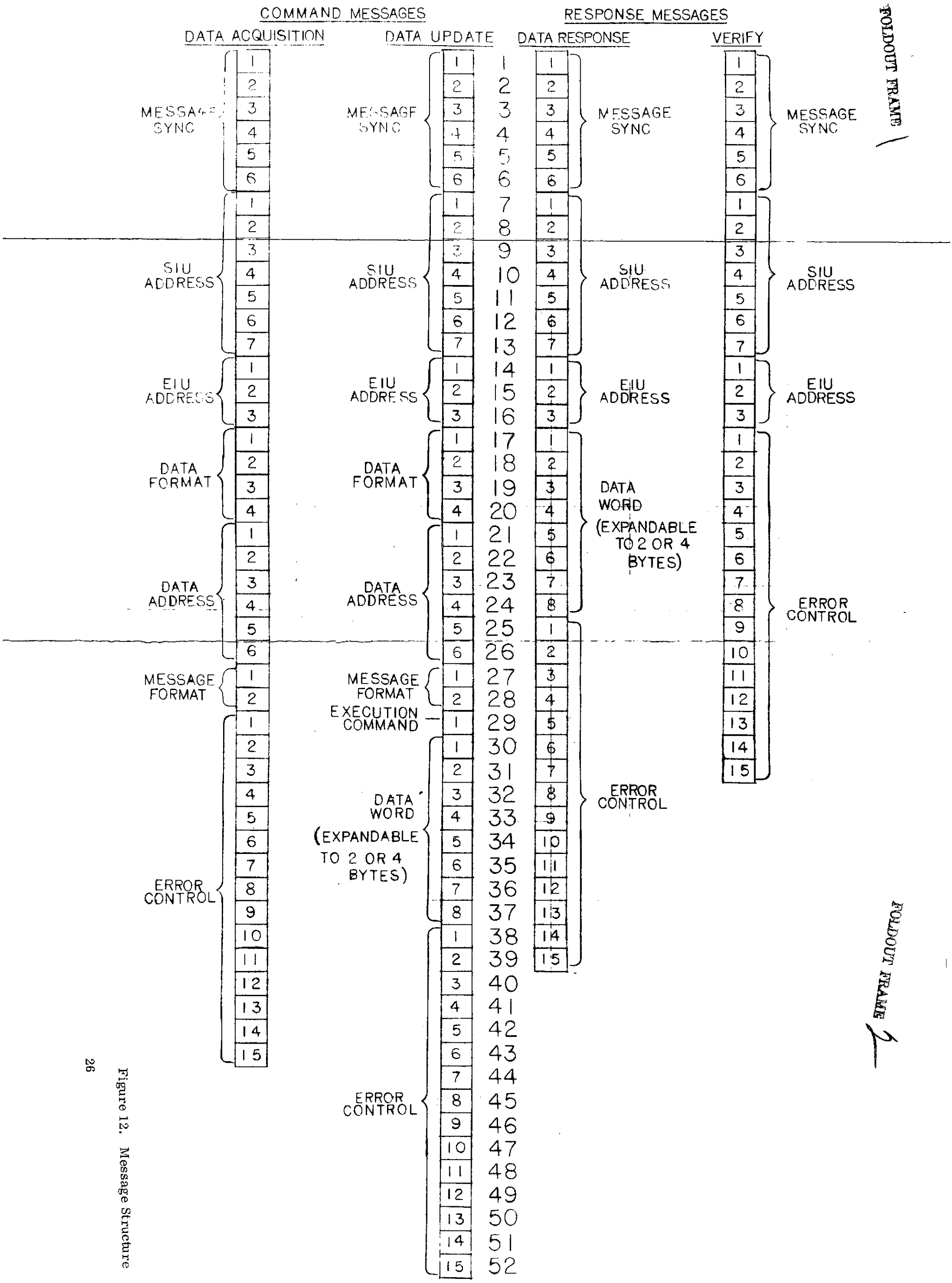


Figure 12. Message Structure

Message Sync

The first six bits of any message are added to the message as it is clocked onto the data bus, and serve to synchronize the timing of the receiving device (EIU or BCU).

SIU Address and EIU Address

The SIU and EIU addresses are a group of 10 bits which provide the message recognition code for only one particular EIU. Each EIU contains an address plug which defines its address as a particular combination of the 10 bits. An EIU will respond to a message only when the SIU and EIU address bits in the command message correspond to the bit pattern defined by its address plug.

By definition, the first seven address bits are referred to as the SIU address and the last three bits are called the EIU address. In system applications, the SIU address would be used to identify EIUs associated with a particular subsystem. The EIU address is used to select one of a number of redundant EIUs which may interface with a given subsystem. In addition to a primary EIU address, which is assigned as a distinct bit pattern for each EIU, there is also a secondary EIU address. Each EIU address plug also defines a secondary EIU address, which would be identical for each EIU associated with a given subsystem. A command message containing the secondary EIU address may be used to simultaneously update all EIUs having that address.

Data Format

The four DATA FORMAT bits are used to select the format of the data to be transmitted from or to the EIU. The standard formats consist of one, two, or four eight-bit bytes. In addition to these, two special formats are defined - ECHO CHECK and STATUS REQUEST. The ECHO format is a one-byte test function; the EIU will respond to an ECHO command message by returning the same data byte in the response message. The STATUS command message is like a one-byte acquisition; the data byte returned in the response message contains information about the status of the EIU (power interrupt, message error).

The bit patterns corresponding to particular DATA FORMAT functions are listed in Table 3.

Table 3. Format Definitions

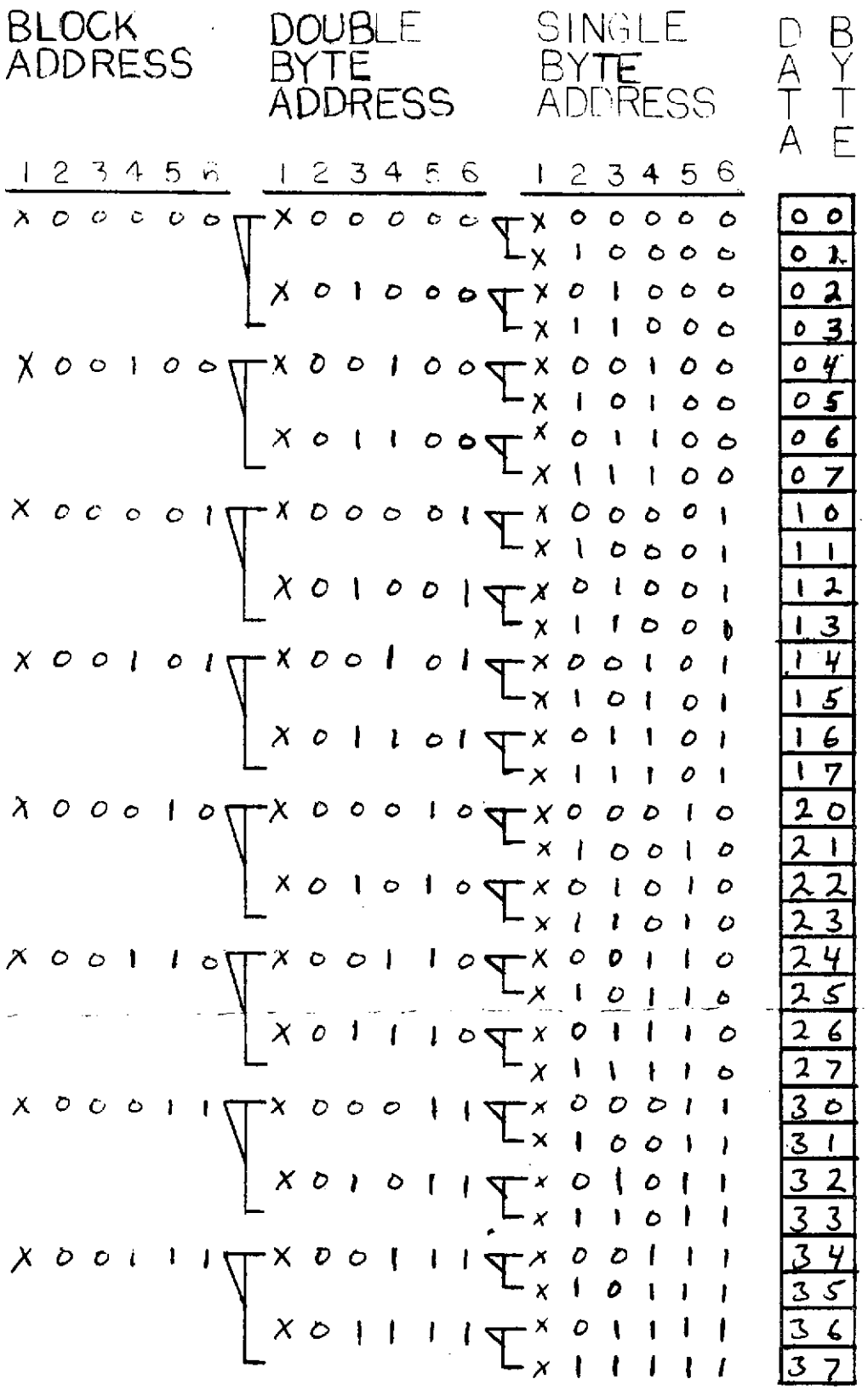
Function	Data	Data Format	Message Format	Response
Digital Update	1 Byte	1001	00	Verify
	2 Byte	1101	00	Verify
	4 Byte	1010	00	Verify
	All (Reset)	1011	00	Verify
Analog Update	1 Byte	1001	01	Verify
	All (Reset)	1011	01	Verify
Digital Acquisition	1 Byte	1001	10	1 Byte Data
	2 Byte	1101	10	2 Bytes Data
	4 Byte	1010	10	4 Bytes Data
	All	1011	10	32 Bytes Data (8 Sequential Transmissions)
Analog Acquisition	1 Byte	1001	11	1 Byte Data
	2 Byte	1101	11	2 Bytes Data
	4 Byte	1010	11	4 Bytes Data
	All	1011	11	32 Bytes Data (8 Sequential Transmissions)
Echo Check	(1 Byte)	1110	11	Echo (1 Byte)
Status Request	(1 Byte)	1100	11	Status Word (1 Byte)

Data Address

The six-bit DATA address is used to indicate which data byte (or group of bytes) is to be accessed in an update or acquisition command. The specific bit patterns used to address each data byte are given in Figures 13 (digital) and 14 (analog). These figures also shown the connection for each data point at the EIU interface.

DATA ADDRESSES — DIGITAL

DIGITAL ACQUISITION —

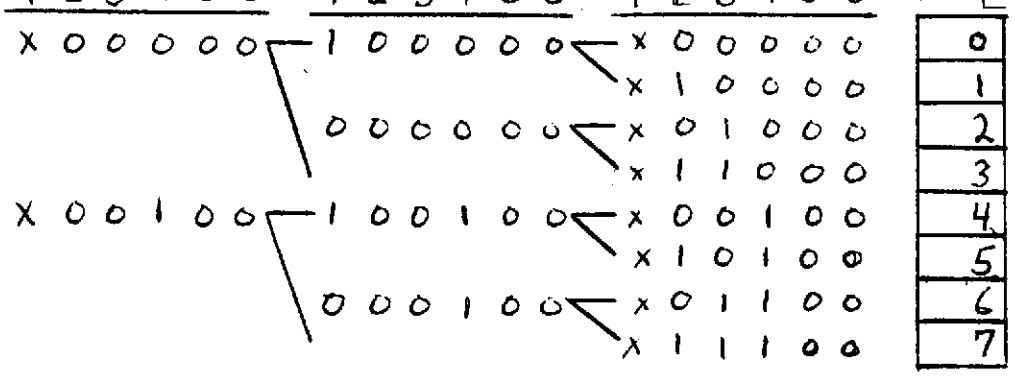


INTERFACE CONNECTIONS —

DATA	SAMPLE INDICATOR
J11-1 THRU 8	J11-10
J11-11 THRU 18	J11-20
J11-21 THRU 28	J11-30
J11-31 THRU 38	J11-40
J11-41 THRU 48	J11-50
J11-51 THRU 58	J11-60
J11-61 THRU 68	J11-70
J11-71 THRU 78	J11-80
J12-1 THRU 8	J12-10
J12-11 THRU 18	J12-20
J12-21 THRU 28	J12-30
J12-31 THRU 38	J12-40
J12-41 THRU 48	J12-50
J12-51 THRU 58	J12-60
J12-61 THRU 68	J12-70
J12-71 THRU 78	J12-80
J13-1 THRU 8	J13-10
J13-11 THRU 18	J13-20
J13-21 THRU 28	J13-30
J13-31 THRU 38	J13-40
J13-41 THRU 48	J13-50
J13-51 THRU 58	J13-60
J13-61 THRU 68	J13-70
J13-71 THRU 78	J13-80
J14-1 THRU 8	J14-10
J14-11 THRU 18	J14-20
J14-21 THRU 28	J14-30
J14-31 THRU 38	J14-40
J14-41 THRU 48	J14-50
J14-51 THRU 58	J14-60
J14-61 THRU 68	J14-70
J14-71 THRU 78	J14-80

FOLDOUT FRAME

DIGITAL UPDATE —



DATA	UPDATE INDICATOR
J11-81 THRU 88	J11-90
J11-91 THRU 98	J11-100
J12-81 THRU 88	J12-90
J12-91 THRU 98	J12-100
J13-81 THRU 88	J13-90
J13-91 THRU 98	J13-100
J14-81 THRU 88	J14-90
J14-91 THRU 98	J14-100

FOLDOUT FRAME 2

X = DON'T CARE

Figure 13. Data Addresses-Digital

DATA ADDRESSES — ANALOG

ANALOG ACQUISITION —

BLOCK ADDRESS 1 2 3 4 5 6	DOUBLE BYTE ADDRESS 1 2 3 4 5 6	SINGLE BYTE ADDRESS 1 2 3 4 5 6	DATA BYTE	INTERFACE CONNECTIONS — DATA POINT HI/LO
X 0 0 0 0 0	X 0 0 0 0 0	X 0 0 0 0 0	00	J10 - 2/1
X 0 0 1 0 0		X 0 0 1 0 0	01	J10 - 4/3
X 0 0 0 1 0	X 0 0 0 1 0	X 0 0 0 1 0	02	J10 - 6/5
X 0 0 1 1 0		X 0 0 1 1 0	03	J10 - 8/7
X 0 0 0 0 1	X 0 0 0 0 1	X 0 0 0 0 1	04	J10 - 10/9
X 0 0 1 0 1		X 0 0 1 0 1	05	J10 - 12/11
X 0 0 0 1 1	X 0 0 0 1 1	X 0 0 0 1 1	06	J10 - 14/13
X 0 0 1 1 1		X 0 0 1 1 1	07	J10 - 16/15
(0 0 0)	X 1 0 0 0 0	X 1 0 0 0 0	10	J10 - 18/17
(1 0 0)		X 1 0 1 0 0	11	J10 - 20/19
(0 1 0)	X 1 0 0 1 0	X 1 0 0 1 0	12	J10 - 22/21
(1 1 0)		X 1 0 1 1 0	13	J10 - 24/23
(0 0 1)	X 1 0 0 0 1	X 1 0 0 0 1	14	J10 - 26/25
(1 0 1)		X 1 0 1 0 1	15	J10 - 28/27
(0 1 1)	X 1 0 0 1 1	X 1 0 0 1 1	16	J10 - 30/29
(1 1 1)		X 1 0 1 1 1	17	J10 - 32/31
(0 0 0)	X 0 1 0 0 0	X 0 1 0 0 0	20	J10 - 34/33
(1 0 0)		X 0 1 1 0 0	21	J10 - 36/35
(0 1 0)	X 0 1 0 1 0	X 0 1 0 1 0	22	J10 - 38/37
(1 1 0)		X 0 1 1 1 0	23	J10 - 40/39
(0 0 1)	X 0 1 0 0 1	X 0 1 0 0 1	24	J10 - 42/41
(1 0 1)		X 0 1 1 0 1	25	J10 - 44/43
(0 1 1)	X 0 1 0 1 1	X 0 1 0 1 1	26	J10 - 46/45
(1 1 1)		X 0 1 1 1 1	27	J10 - 48/47
(0 0 0)	X 1 1 0 0 0	X 1 1 0 0 0	30	J10 - 50/49
(1 0 0)		X 1 1 1 0 0	31	J10 - 52/51
(0 1 0)	X 1 1 0 1 0	X 1 1 0 1 0	32	J10 - 54/53
(1 1 0)		X 1 1 1 1 0	33	J10 - 56/55
(0 0 1)	X 1 1 0 0 1	X 1 1 0 0 1	34	J10 - 58/57
(1 0 1)		X 1 1 1 0 1	35	J10 - 60/59
(0 1 1)	X 1 1 0 1 1	X 1 1 0 1 1	36	J10 - 62/61
(1 1 1)		X 1 1 1 1 1	37	J10 - 64/63

ANALOG UPDATE —

SINGLE 1 2 3 4 5 6	DATA BYTE	DACON OUTPUT HI/LO
X 0 0 0 0 0	0	J10 - 66/65
X 1 0 0 0 0	1	J10 - 68/67
X 0 1 0 0 0	2	J10 - 70/69
X 1 1 0 0 0	3	J10 - 72/71
X 0 0 1 0 0	4	J10 - 74/73
X 1 0 1 0 0	5	J10 - 76/75
X 0 1 1 0 0	6	J10 - 78/77
X 1 1 1 0 0	7	J10 - 80/79

X = DON'T CARE

FOLDOUT FRAME

FOLDOUT FRAME 2

Figure 14. Data Addresses - Analog

Message Format

The two-bit MESSAGE FORMAT is used to select the function to be performed by a command message. The first bit is used to select update (0) or acquisition (1); the second bit selects digital data (0) or analog data (1). The defined uses of the MESSAGE FORMATS in conjunction with various DATA FORMATS are shown in Table 3. It should be noted that the STATUS and ECHO functions require a MESSAGE FORMAT of "11".

Execution Command

The EXECUTION COMMAND bit is used only in conjunction with an update command message. If this bit is 0, the update data is held in the EIU, but does not appear at the interface. If the bit is 1, the update data is routed to the interface.

Data Words

The DATA WORDS which appear in data update command messages and data response messages consist of one, two or four data bytes (each eight bits in length), depending on the DATA FORMAT.

Error Control

The last 15 bits of all messages consist of ERROR CONTROL information. These bits are generated for outgoing messages and checked on oncoming messages to provide for cyclic error detection on all data bus messages.

Bus Exerciser Control Panel

As shown in Figure 2, the Bus Exerciser control panel is divided into two main functions: MESSAGE TRANSMIT and MESSAGE RECEIVE. MODE and POWER controls are located at the lower right corner.

The MESSAGE TRANSMIT section of the Bus Exerciser control panel is used to define the transmitted message, and to provide for initiating and controlling its transmission on the data bus.

The message switches consist of the SIU ADDRESS; EIU ADDRESS DATA FORMAT; DATA ADDRESS MESSAGE FORMAT; EXECUTION COMMAND; four DATA BYTES; and the ERROR CONTROL word. Under each of the bits of the message, a lamp and toggle switch are provided. These switches are used for setting the message, and the lamps are used to read the loaded or transmitted message.

In the lower left-hand corner of message transmit are the BUS CONFIGURATION switches. They provide the capability of sending the loaded message down any channel to the EIUs. The OPERATION switch provides either single-step or repetitive operation; that is, a cyclic program stored within the computer allows either a single-step or repetitive transmission to be requested. The MESSAGE SELECT switch allows the operator to select the channel to be loaded and displayed.

The FORMAT ERROR lamp is illuminated when a format error is detected by the computer. This may result from an undefined MESSAGE FORMAT being set in the switches, or an improper sequence of actuation of the control switches by the operator.

The COMPUTER READY lamp indicates the status of the computer, and TRANSMISSION IN PROCESS lamp indicates whether a transmission is taking place down a data bus.

The PROGRAM LOAD AND ERROR CHECK pushbutton switch loads the settings from the message switches, exclusive of the ERROR CONTROL switch settings. This initiates the cyclic error control calculation within the computer. Upon completion of the calculation, the appropriate ERROR CONTROL lamps are illuminated. The illuminated lamps indicate the proper error control word for the message set on the switches above.

The LOAD pushbutton switch reads the settings of the message switches into the computer, and performs the necessary formatting and control functions to prepare the message for transmission on the data bus. The method of loading the error control bits is dependent on the setting of DATA switch "O" (DO) in the NOVA front panel. If the DO switch is down (O), the error control bits for the transmitted message are read in from the ERROR CONTROL switches on the front panel. This "manual" mode allows an incorrect error control bit to be transmitted for test purposes. If the NOVA DO switch is up (1), the error control bits are added to the transmitted message as they appear in the ERROR CONTROL lights. With no reference to the switches, this "automatic" mode allows for faster and easier setup and transmission of messages when corrector error control is required.

The TRANSMIT switch initiates the transmission of the loaded message down the selected data bus. The TRANSMISSION HALT switch terminates all transmissions from bus exerciser to EIUs.

The MESSAGE RECEIVE section of the Bus Exerciser control panel provides indicator lights and operational controls to display data bus response messages. The terms "accepted" and "selected" relate to redundant operation, and therefore are not meaningful for DBS-II. The ANALOG ACCURACY switch is not used in DBS-II.

The received messages are displayed in the following manner. The first seven address bits (defined as the SIU ADDRESS) are displayed under SIU ADDRESS in the ACCEPTED DATA BUS MESSAGE lights. The last 3 address bits (defined as the EIU ADDRESS) are displayed under SIU ADDRESS in the SELECTED DATA BUS MESSAGE lights. The SELECTED MESSAGE lights are used for the remainder of the message. Data bits (if present) will appear in the DATA BYTE 1, 2, 3, or 4 sections. The error control bits will appear in the ERROR CONTROL lights.

The DATA BUS ERROR lamps indicate when an error is detected on a particular channel, provided the ERROR INTERRUPT switch is in the ENABLE position. If that switch is in the DISABLE position, no DATA BUS ERROR lamps will be illuminated. In addition to enabling or disabling the error lamps, the ERROR INTERRUPT switch will stop the message when

the OPERATION switch is in the REPETITIVE mode and the ERROR INTERRUPT switch is in the ENABLE mode. When the ERROR INTERRUPT switch is in the DISABLE mode, the message is under computer control for repetitive cycling of message.

The DISPLAY LAST RESPONSE switch, in conjunction with the SELECT DATA BUS DISPLAY switch, displays the response message from the selected channel.

The RESPONSE MESSAGE INCREMENT switch, in conjunction with the SELECT DATA BUS DISPLAY switch and subsequent to actuation of the DISPLAY LAST RESPONSE, will sequentially display on the SELECTED DATA BUS MESSAGE the multiple response messages from the SIUs.

The DISPLAY TRANSMITTED MESSAGE switch, in conjunction with the TRANSMIT MESSAGE SELECT, displays the appropriate transmit message on the upper panel.

The COMPUTER CONTROL and OPERATOR CONTROL switches provide the option of computer or operator message control.

The RESET switch presets and clears the logic in the Bus Exerciser.

The ON-OFF power switch controls +12 vdc and -15 vdc power to the Bus Exerciser.

The DATA BUS 1/DATA BUS 2 switch determines the operational configuration of the Bus Exerciser. In the DATA BUS 1 position, the Bus Exerciser operates in the original mode, using internal transceivers to interface with the data bus. This switch position should be used when the Bus Exerciser is used with DBS-II units; the NOVA DATA switch 1 (D1) should be placed in the up position. In this mode, all operation is the same as DBS-I except that redundant operation is not possible.

With the DATA BUS switch in the DATA BUS 2 position, the Bus Exerciser will operate with the DBS-II hardware (SIU-s, EIUs and BCUs). In this mode of operation, the Bus Exerciser interfaces with the data bus via BCU's. These units also provide time slots, which are

compared by circuitry in the bus exerciser to detect error. The time slots are used to gate transmissions out of the Bus Exerciser. The TIME SLOT switch selects either voted time slot gating (TSV position) or "A" time slot gating (TSA position). In order to achieve continuous transmissions with DBS-II, the BCU MESSAGE FORMAT switches should be placed in the CW position.

Equipment Initiation

To energize the Data Bus System, proceed as follows:

(1) On the Bus exerciser front panel, on the +5 VDC Bus Exerciser power supply, and on the minicomputer place the power switch to the ON position, in the order specified.

(2) On the teletypewriter, place the LINE/LOCAL switch to LINE.

(3) Apply +28 vdc power to the EIUs and SIUs.

Operational Procedure (Typical)

To operate the Data Bus System, proceed as follows, assuming an operational programis resident in minicomputer (for program loading procedures, refer to Table 4):

(1) On the minicomputer, set the ADDRESS switches to 07600.

(2) Actuate the minicomputer RESET switch.

(3) Actuate the minicomputer START switch.

(4) On the Bus Exerciser, actuate the RESET switch.

(5) On the Bus Exerciser, actuate the OPERATOR CONTROL.

(6) Set the BUS CONFIGURATION switch for the desired channel.

(7) Set the OPERATION switch for SINGLE STEP or REPETITIVE transmission. Set the ERROR INTERRUPT switch to ENABLE or DISABLE, as desired.

Table 4. Computer Loading Procedure

(1) Using the front panel switches, enter the Bootstrap Loader as follows:

Location	Coding
7757	126550
7760	63610
7761	777
7762	60510
7763	127100
7764	127100
7765	107003
7766	772
7767	1400
7770	60110
7771	4766
7772	44402
7773	4764

(2) Put the Binary Loader tape in the TTY reader. Enter 7770 in the data switches. Raise the START switch. Program will load.

(3) Put the long black tape labelled "Data Bus System II" in the TTY reader. Enter 7777 in the data switches. Raise the START switch. The tape will load to completion.

(4) Raise the START switch again (this loads the patch at end of tape).

(5) Repeat the paragraph 3 procedure, using the tape labelled "Debug II".

(6) To execute the Data Bus program, set the data switches to 7600 and raise the START switch.

(7) If the use of the Debug II program is desired, set the DATA switches to 6200, insert breakpoints, etc., and type: 7600R.

Table 4. Computer Loading Procedure (Cont)

Program Patch:

Location	Old Contents	New Contents
1324	41454	41455

(8) Set the desired message (i.e., SIU ADDRESS, EIU ADDRESS, DATA FORMAT, DATA ADDRESS, MESSAGE FORMAT, EXECUTION COMMAND, and DATA BYTES). An up position of a switch is a logic "1".

(9) Actuate the PROGRAM LOAD AND ERROR CHECK switch. Corresponding message lamps should light, including the appropriate ERROR CONTROL.

(10) In order to transmit a correct message, place the NOVA "DATA O" switch in the up position.

NOTE: Message may be modified prior to each loading.

(11) To load one or more channels individually set the MESSAGE SELECT switch to desired channel and actuate the LOAD switch. Repeat for each channel.

(12) Actuate the TRANSMIT switch. (If the OPERATION switch is in the REPETITIVE position, repeated transmissions will occur. If in the SINGLE STEP position, only one transmission will occur.)

(13) Actuate the TRANSMISSION HALT switch when desired. This completes the transmission operation.

(14) Set the SELECT DATA BUS DISPLAY switch to the desired channel.

(15) Actuate the DISPLAY LAST RESPONSE switch. Observe the ACCEPTED/SELECTED DATA BUS MESSAGE lamps for the received message. If there is more than one received message, actuate the RESPONSE MESSAGE INCREMENT switch for all EIU response messages for that particular transmission.

NOTE: Repeated observation of messages may be attained by actuating the DISPLAY LAST RESPONSE switch and RESPONSE MESSAGE INCREMENT switch again.

(16) For observation of messages on other SELECT DATA BUS DISPLAY positions, repeat steps (14) and (15).

(17) To transmit/receive a new message, repeat steps (4) through (16).

SOFTWARE

In normal operation, the information set into the MESSAGE TRANSMIT switches (excluding the error control bits) is read into the computer. The message format and data format bits are analyzed by the computer to determine the type of message that is to be transmitted. The message bits are then formatted for loading into the output registers of the Bus Exerciser. During this operation, the appropriate error control bits are determined and added to the message. At this point, the operator has the option to insert incorrect error control bits into the message, to test the operation of the error check circuitry in the Data Bus hardware. The program also sets up parameters in the software routines and various hardware registers as necessary for the transmission of the message, and read in and display of the resulting response message(s).

The transmission of the message on the bus is initiated by the operator. Depending on the setting of various front panel switches, the message may be transmitted on any combination of the four output channels, and may be sent once, or repeated until terminated by the operator. When the response message is received, it is automatically read into the computer under program control, and can subsequently be formatted for display on the front panel lights. In the continuous mode, the last message received after transmission is halted and displayed. During redundant operation, the several responses are compared using a majority voting routine, and incorrect messages are rejected. In this mode, individual responses and/or the "correct" response may be displayed.

In conjunction with the design and construction of the Data Bus Systems, computer programs were developed to allow operation of the system hardware under operator direction. The programs reside in the Bus Exerciser minicomputer, and supervise the transmission and reception of all types of messages on the Data Bus. The primary purpose of the programs is to provide for manual generation of messages for use in integration and testing of the system.

The major portion of the software was developed during the first phase of the Data Bus effort, and provided the capabilities necessary to exercise the DBS-I hardware functions. As further development of the Data Bus concept led to the SIU-P system and DBS-II, the programs were modified and expanded to accommodate the added functions. Also a program was developed to operate in the preprocessor (minicomputer) to test its operation in conjunction with the SIU-P.

Data Bus System I Program

The DBS-I program includes all major program routines necessary to set up, load, transmit, receive and display all the various formats of Data Bus messages. Message bits (addresses, formats, data words, etc.) are set up using the front panel data switches; loading, formatting, transmission, display and other operations are performed by various program routines which are activated by front panel function switches.

During the operation of all routines, the programs perform checks for various types of errors, and provide indications on the front panel lights if errors are detected. The major kinds of errors which are identified include entering undefined Data Formats, improper actuation sequence of function switches, missing response messages, and incorrect error control bits in response messages.

The Data Bus programs are designed to allow rather detailed control of all functions by the operator. While this approach does not demonstrate by any means the full potential of the computer in automatic handling of Data Bus traffic, it does provide the flexibility of control necessary for efficient integration and testing of the Data Bus System. Utilizing the Bus Exerciser programs, all of the data handling, error detection and self test features of the system can be demonstrated, including the high data rates which may be achieved.

Detailed information on the DBS-I program is contained in the Operation and Maintenance Manual - Data Bus System 1. This information includes operational procedures, program descriptions, and computer listings for all routines.

SIU-P and Preprocessor Programs

With the modification of the SIU design to include interface with a preprocessor (minicomputer), additional software was developed. Several additional capabilities were integrated into the DBS-I program. A routine was generated which allowed blocks of data words to be loaded from the Bus Exerciser minicomputer into the preprocessor via the Data Bus and SIU-P. Two variations of the basic routine were provided; the first of these is used to clear a predefined area in the preprocessor memory (by loading zeroes). The other routine takes a block of program instructions, initially resident in the Bus Exerciser computer, and loads it into preprocessor memory in the same manner. These instructions may then be executed as a program in the preprocessor.

Another program routine was developed to extend the capability of the Bus Exerciser to include the transmission of messages containing commands to control the operation of the preprocessor. The preprocessor control functions included load, examine, start and halt. The preprocessor loading and control command routines were designed to be fully automatic, requiring only initiation by the operator, since they were intended to perform very specific functions.

Utilizing these routines, programs can be loaded into the preprocessor and initiated. A group of preprocessor programs was generated which demonstrated the various capabilities of the preprocessor, operating in conjunction with the SIU-P. These capabilities include updating and acquisition of data at the subsystem interface, manipulation of data, and return of processed subsystem data to the Bus Exerciser.

Detailed information on the SIU-P and Preprocessor software is contained in the Operation and Maintenance Manual - Data Bus System I - SIU-P and Preprocessor. This information includes operational procedures, SIU-P-Preprocessor programming instructions, and program descriptions and listings.

Data Bus System II Program

The majority of the DBS-II Program is identical to the DBS-I Program (excluding the SIU-P - Preprocessor capabilities). Modifications were made to accommodate additional functions and expanded addressing. Minor additions were incorporated to handle an added data format and expanded data responses. The routines dedicated to formatting of response messages for display were modified to accommodate the EIU address bits in addition to the SIU address.

The changes to the program were designed to allow for compatibility with either the DBS-I or DBS-II hardware units. The software can be configured to operate with either system by changing the position of a data switch on the front panel of the Bus Exerciser minicomputer.

Operational procedures, program descriptions, flow charts and listings for the DBS-II program can be found in the Operation and Maintenance Manual - Data Bus System II.

STUDIES

Seven different but related studies were completed as a part of the Data Bus System program:

1. BCU Requirements
2. Redundancy Interface
3. SIU/Preprocessor Interface
4. Logic Levels
5. Integrated Diagnostics Performance
6. Self-Powered Data Bus
7. ARINC Compatibility

BUS CONTROL UNIT REQUIREMENTS STUDY DRL LINE ITEM NUMBER 4

The analysis identified job task structure between the Bus Control Units and the central computers. The RCA 215 central computer was used since it is considered representative of the computers under consideration by NASA.

The following design trade-offs with conclusions and recommendations are discussed in the report.

1. Error Code Generation and Checking
2. Preflight Checkout
3. Bus Traffic Control
4. Transfer of Small and Large Data Blocks
5. Data Distribution
6. Limit Checks
7. Voting and Cross-Strapping

The report also contains a BCU block diagram with a description reflecting the results of the study.

DATA BUS SYSTEM/VEHICLE SUBSYSTEM INTERFACE-REDUNDANCY INTERFACE ANALYSIS DRL LINE ITEM NUMBER 6

The analysis considered the problem of interfacing a quad-redundant data bus with vehicle subsystems having fewer than four levels of redundancy. This interfacing should be accomplished while maintaining completely isolated SIU's and premitting the vehicle subsystem to communicate with the DMS subsystem over all the data bus redundant paths. In addition, interface techniques, relative reliability exhibited by the SIU and subsystem I/O's , and failure propagation from SIU to SIU are discussed.

Conclusions were drawn based on an analysis of two connection schemes (cross-strapping and mini-bus) and on relative subsystem reliability. The report recommends that the mini-bus approach be implemented for a non-redundant vehicle subsystem interfacing and final flight models of SIU's should incorporate failure propagation protection circuitry.

SIU/PREPROCESSOR INTERFACE STUDY-DRL LINE ITEM NUMBER 5

This study defines the relationship between the Data Bus Subsystem Interface Unit and the NASA selected Preprocessor, the Data General NOVA 1200.

It was recognized that the problem of certain subsystems hogging a redundant data bus due to excessive I/O traffic could be alleviated by augmenting an SIU with a local computer - that is, a preprocessor. The report discusses the advantages of such a preprocessor and contains block diagrams and the description of the system utilizing the NOVA 1200 and the SIU.

SIU/VEHICLE SUBSYSTEM INTERFACE - LOGIC LEVEL ANALYSIS DRL LINE ITEM NUMBER 7

The logic interface between the SIU and the shuttle subsystem is analyzed in detail in terms of signal levels, and noise margins and noise susceptibilities. The principal sources of noise which are considered are cross-talk between adjacent lines and transmission-line effects.

The conclusion of the report is that the existing design is acceptable and that operating safety margins are sufficient. A recommendation is made as to specific cabling to be used for the SIU/Shuttle subsystem digital signal wiring.

INTEGRATED DIAGNOSTICS PERFORMANCE ANALYSIS
DRL LINE ITEM NUMBER 32

The requirement for this study was to take a detailed look at the signal levels, signal type, signal quantity, and timing requirements of each subsystem addressed by the NAS9-11189 report. The NAS9-11189 report is the engineering study of on-board checkout techniques written by IBM.

This study was to ascertain how the RCA Data Bus hardware and the IBM DMS study recommendations can be merged. This report details the comparisons between RCA and IBM approaches with suggestions for future design decisions.

SELF POWERED DATA BUS
DRL LINE ITEM NUMBER 28

This study was concerned with the practicality and feasibility of using DBS-II for applying power to remote terminal EIU's and SIU's in addition to providing the transmission medium for BCU to remote terminal communications.

Results of the study indicate that it is neither practical nor feasible to have a self-powered data bus. However, substantial power savings can be realized by operating the EIU's in a standby mode. The principal problem with a self-powered data bus is the inability of the Twinax cabling to handle the high power requirements of multiple redundant remote terminal configurations.

ARINC COMPATIBILITY STUDY
DRL LINE ITEM NUMBER 33

The purpose of this study was to compare RCA data bus design with the data bus described in ARINC characteristic 575-3. Major differences were identified and changes necessary to make the systems compatible were determined. The impact of the required changes on the Data Bus System's operational characteristics was also determined.

The result of the study was that any attempt at making the RCA Data Bus System as designed to the NASA Scope of Work compatible with ARINC characteristic 575 would result in a system that does not meet the specified operational requirements.

DOCUMENTATION

Principal documents developed under the contract were of four types; test procedures, test reports, task reports, and operation and maintenance manuals.

Test Procedures

The test procedures prepared by RCA for acceptance and qualification of the Data Bus Systems included the following:

Data Bus System I	- Item 16, TM-099T
SIU/Preprocessor Interface	- Item 17, TM-099T
Data Bus System II	- Item 25, TM-099T

Acceptance Test Procedures

Acceptance test procedures were written for the following three systems:

1. Data Bus System I - SIU
2. Data Bus System I - SIU/P
3. Data Bus System II - SIU, EIU, and BCU

Each procedure defines the acceptance testing required to ensure that each Bus System operates in accordance with the requirements specified in the NASA Statement of Work for the Data Bus System Development.

Bus System I - Subsystem Interface Units/Preprocessor

The acceptance of each unit depended on satisfactory demonstration that the SIU conform to the requirements specified in the Statement of Work for Message Role, Analog and Digital Data Acquisition, Analog and Digital Distribution, and Initialization. The SIU's are required to demonstrate the system capability to operate in both a simplex and a redundant (FO-FO-FS) manner.

Bus System I - Subsystem Interface Units/Preprocessor

The acceptance of each SIU depended on satisfactory demonstration that the SIU/P conform to the requirements specified in the Scope of Work and/or Message Role, Analog and Digital Data Acquisition, Analog and Digital Distribution and Initialization. The SIU/P's are required to demonstrate the system capability to operate in a simplex manner.

Bus System II - Standard Interface Units, Electronic Interface Units, and Bus Control Units

The acceptance of each EIU depended on satisfactory demonstration that each unit conform to the requirements specified in the Scope of Work for Message Role, Analog and Digital Data Acquisition, Analog and Digital Distribution and Initialization. The SIU/S's are required to demonstrate the capability to interface eight transmit/receive channels with the data bus, and to generate synchronized time slots. The capability of the Bus Exerciser to compare the time slot signals from four BCU's and to use a voted time slot signal to gate the data bus transmissions is also required.

Test Reports

Acceptance test data sheets were made for each unit or chassis tested during qualification sell-off. The qualification test report was prepared at the completion of each phase of testing. The following reports were prepared by RCA:

Data Bus System I	- Item 18, TM-100T
Data Bus System II	- Item 26, TM-100T
SIU/Preprocessor Interface	- Item 29, TM-100T

Operation and Maintenance Manuals

Operation and maintenance manuals have been written for Data Bus Systems I and II. These manuals cover the description, installation, operation, theory and the general maintenance of the systems.

Data Bus System I	- Item 30, OM-008T
Data Bus System II	- Item 27, OM-008T

Task Reports

The Data Bus System development program includes task reports written for the seven completed studies.

Bus Control Unit	- Item 4, SE-351T
Redundancy Interface	- Item 6, SE-351T
SIU/Preprocessor Interface	- Item 5, SE-351T
Logic Level	- Item 7, SE-351T
Integrated Diagnostics Performance	- Item 32, SE-351T
Self-Powered Data Bus	- Item 28, SE-351T
ARINC Capability Study	- Item 33, SE-351T

MECHANICAL DESIGN

All the electronic hardware delivered under this contract was packaged as engineering models. The equipment is suitable for operation in a normal laboratory environment without special cooling provisions and permits maintenance and repair at the user's facility with normal laboratory equipment. The basic packaging design makes use of Augat Series 8136-U high density packaging panels. These are interconnected by a wire wrapped backplane assembly and contained within a sheet metal enclosure which may be located upon a flat surface. The enclosure has removable top and bottom covers, permitting both card removal and access to the backplane wiring. Each card provides plug-in mounting for sixty dual-in-line (DIP) micro-electronic components. Interconnections among the DIP's and the edge on connector are accomplished by coil wrap.

The high frequency circuits, in general, use discrete components, as opposed to DIP's and require circuit connection lengths to be minimal. These circuits were, therefore, packaged using double sided printed boards with the components soldered in place.

Since the Bus Exerciser will not be required as flight hardware, it was packaged for mounting in the standard 19" equipment rack used in the Bus Exerciser System. The unit contains two wire wrapped basket assemblies for Augat cards and is mounted in the rack by means of the front panel and slide assemblies. The slides permit access to the boards and the backplane wiring for maintenance.

Data Bus System I

The DBS-I consists of the equipment listed in Table 5.

Table 5. Data Bus System I Equipment

Equipment	Quantity
Bus Exerciser Set	1
Bus Cable Set	4
SIU	16
SIU-P	8

The equipment is shown in Figure 3.

Data Bus Exerciser Set

All units except the Teletypewriter are mounted in a standard 19" equipment rack whose outline dimensions are 25-1/2 wide x 50-9/16 high x 24-5/16 deep.

The Teletypewriter, Minicomputer and +5 VDC Power Supply are commercial equipment as described in the Operational and Maintenance Manual.

The Bus Exerciser is a rack mounted chassis containing plug-in Augat cards. The location of these cards within the chassis is shown in Figure 15. Outline dimensions for the unit are provided in Figure 16.

The blower assembly provides adequate circulation of room ambient air within the rack to assure satisfactory operation of the rack electronics.

Bus Cable Set

A Bus Cable Set consists of the cable and accessories necessary to construct a Data Bus channel. The equipment includes: Twinax cable assemblies, power dividers, and line terminations.

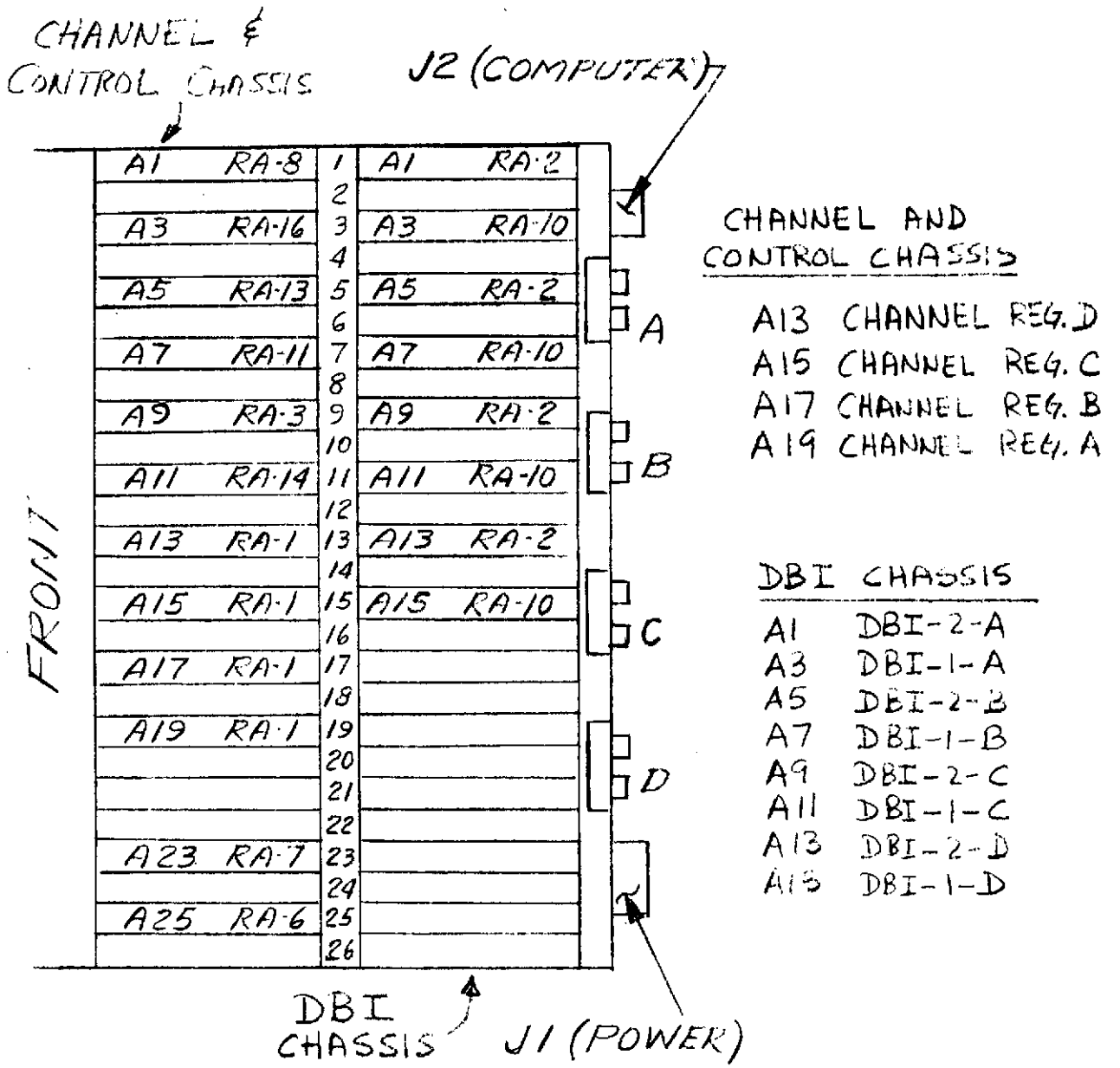


Figure 15. Bus Exerciser, Board and Connector Locations

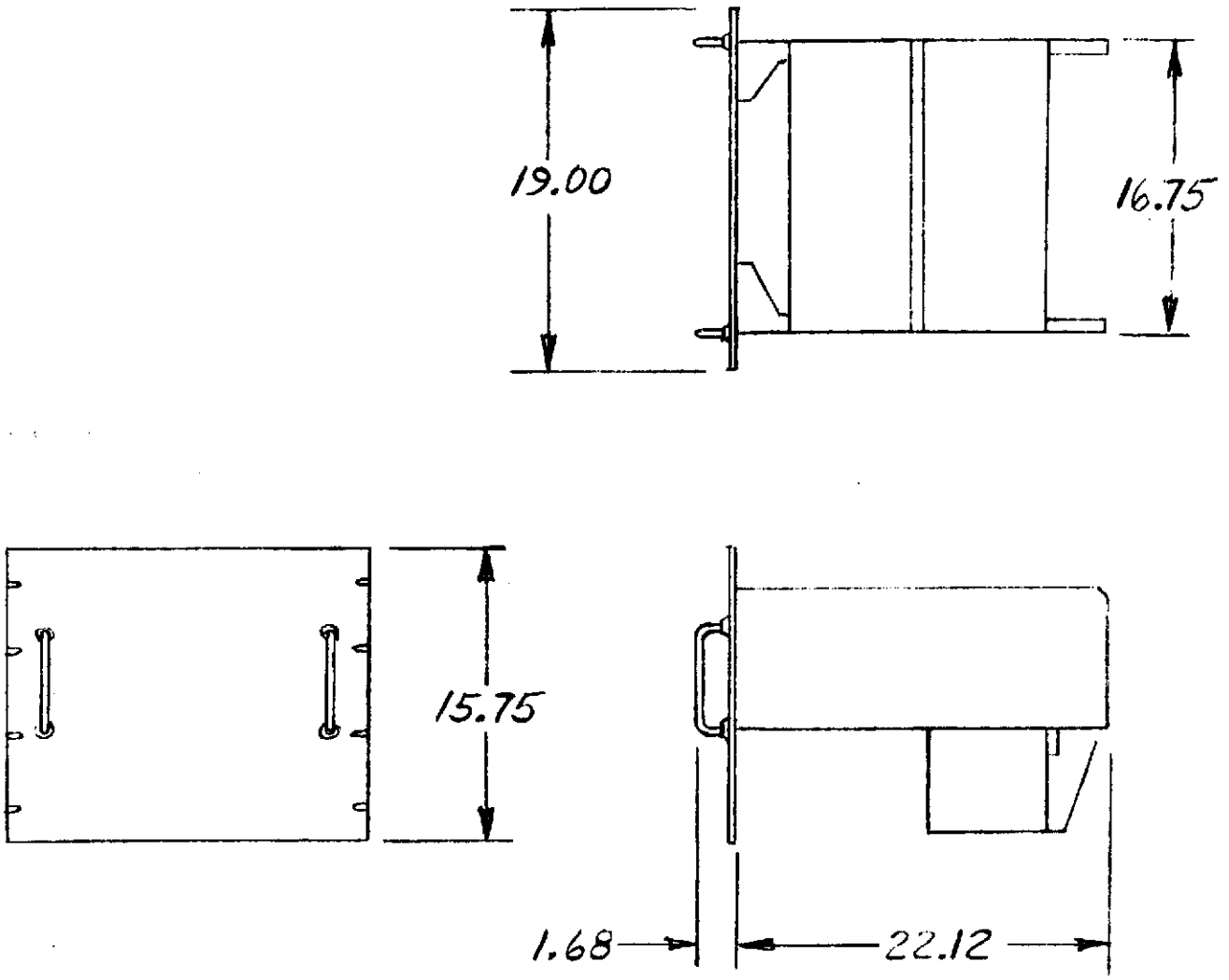


Figure 16. Bus Exerciser Overall Dimensions

The three types of data bus remote terminals developed, the SIU, the SIU-P, and the EIU, along with the two bus exercisers and BCU's all were fabricated on Augat printed circuit boards with plug-in TTL and COS/MOS microelectronic circuitry. The PC boards are labelled RA-1 through RA-25 with the individual unit board complement summarized in Table 6, and are positioned in basket-type frames to provide the breadboard flexibility required by NASA.

Subsystem Interface Unit

The SIU is constructed in accordance with the basic packaging technique. Outline dimensions are shown in Figure 17 and the location of major assemblies in Figure 18.

The power supply is a potted commercial unit described in the O&M Manual. The Transceiver Unit consists of a printed board assembly mounted within an RF tight box. Ten plug-in wire wrapped boards are used.

Subsystem Interface Unit with Preprocessor (SIU-P)

This set of equipment consists of: a modified SIU and preprocessor interface assembly which is interchangeable with and mounts in place of the NOVA 1200 minicomputer front panel; and the necessary cabling.

The SIU modifications involve: replacement of two boards (RA12, RA15) and the inclusion of an additional board (RA17). The preprocessor front panel assembly is shown in Figure 19.

Data Bus System II

The DBS-II consists of the equipment listed in Table 7:

Table 6. PC Board Complement

Type	Name	Quantity SIU	SIU-P	EIU	BCU	Exerciser
RA-1	Channel Register (A, B, C, D)					4
RA-2	Data Bus Interface No. 2	1	1	1		4
RA-3	Bus Configurator and Shift Delay					1
RA-4	Analog Acquisition	1	1	1		
RA-5	Digital Acquisition	1	1			
RA-6	Display Storage Register					1
RA-7	Switching and Interrupt Multiplexer					1
RA-8	Computer Interface					1
RA-9	Data Distribution	2	2	2		
RA-10	Data Bus Interface No. 1	1	1	1		4
RA-11	Transmit and Receive Switching					1
RA-12	Sequence Controller No. 1	1				
RA-12P	Sequence Controller No. 1		1			
RA-13	Address and Word Counter					1
RA-14	Computer Data Input					1
RA-15	Sequence Controller No. 2	1				
RA-15P	Sequence Controller No. 2		1			
RA-16	Message Receive and Time-Out Counter					1
RA-17	Preprocessor Interface		1			
RA-18	Front Panel Interface No. 1		1			

Table 6. PC Board Complement (cont)

Type	Name	Quantity SIU	SIU-P	EIU	BCU	Exerciser
RA-19	Front Panel Interface No. 2		1			
RA-20	Digital Acquisition			4		
RA-21	Sequence Control Unit No. 1			1		
RA-22	Sequence Control Unit No. 2			1		
RA-23	Data Bus No. 2 Interface					*1
RA-24	Clock Generator				1	
RA-25	Time Slot Generator				1	
	Totals	8	11	11	2	20/21*

*Data Bus 2 Exerciser

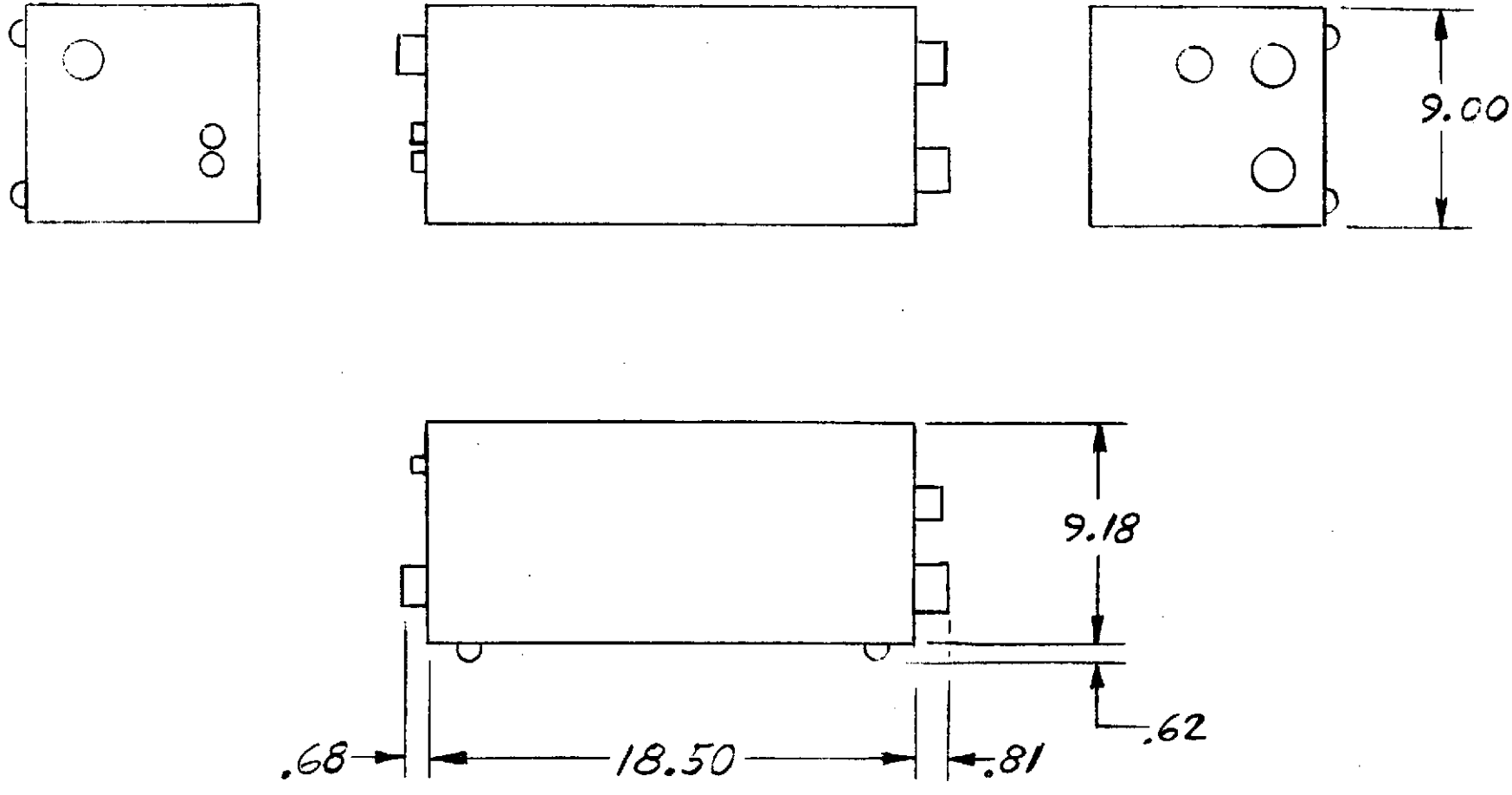


Figure 17. SIU Overall Dimensions

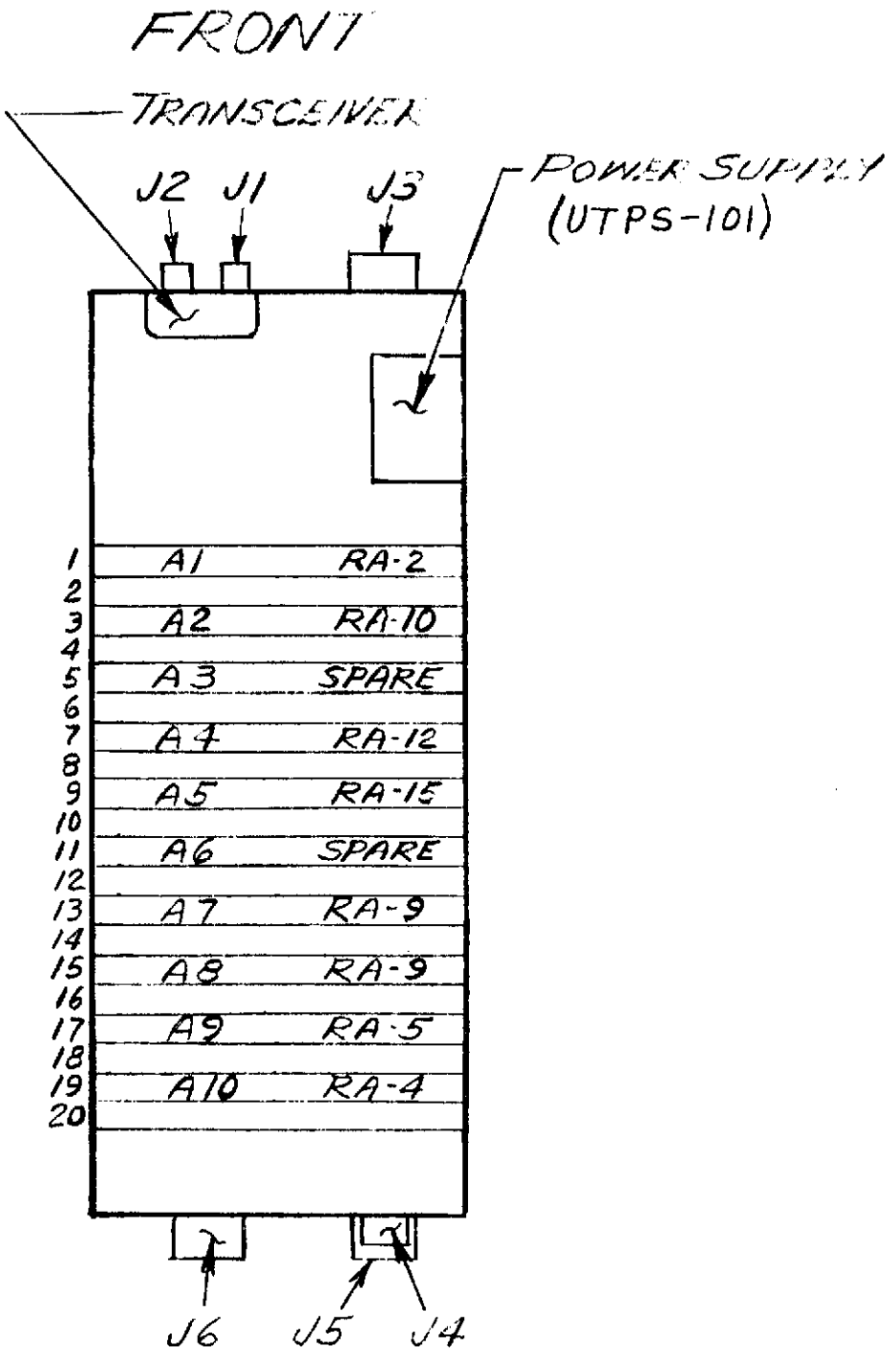
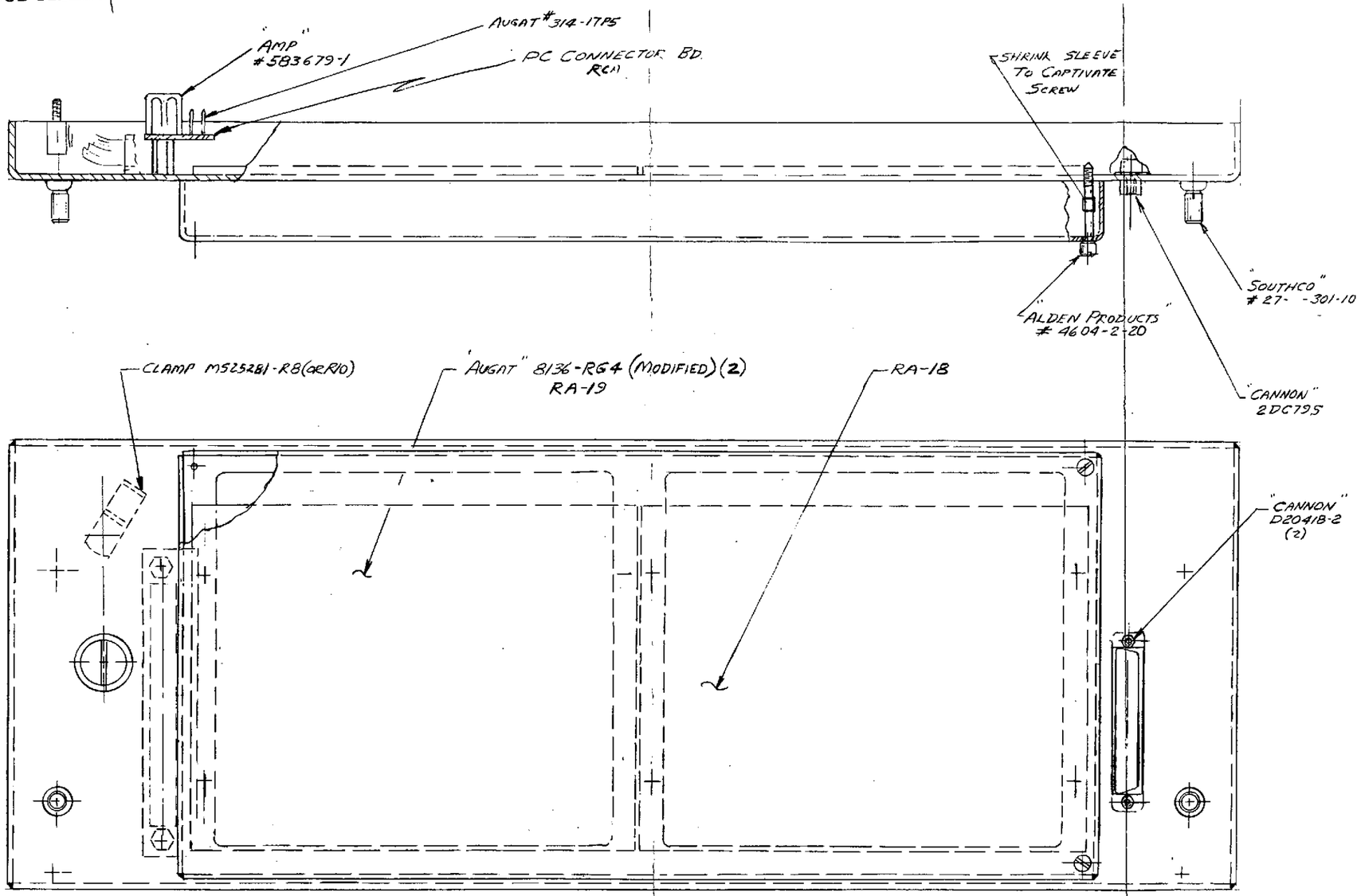


Figure 18. SIU, Board and Connector Locations

FOLDOUT FRAME

FOLDOUT FRAME 2



FRONT-END MODIFICATION FOR NOVA 1200

Figure 19. Mechanical Drawings for SIU-P Preprocessor (Nova 1200) Front Panel

Table 7. Data Bus System II Equipment

Equipment	Quantity
BCU	4
SIU-S	12
EIU	8
Bus Cable Set	4
Bus Exerciser Set	1

Bus Control Unit

The BCU, shown in Figure 20, contains two Augat cards, on printed board assembly and several power supplies. Accessibility to all assemblies is provided by removal of the cover. Outline dimensions of the unit are 9 x 4 x 11-3/8.

Standard Interface Unit - Serial

The SIU-S shown in Figure 21 consists of a printed board assembly and two power supplies contained within an RF tight enclosure.

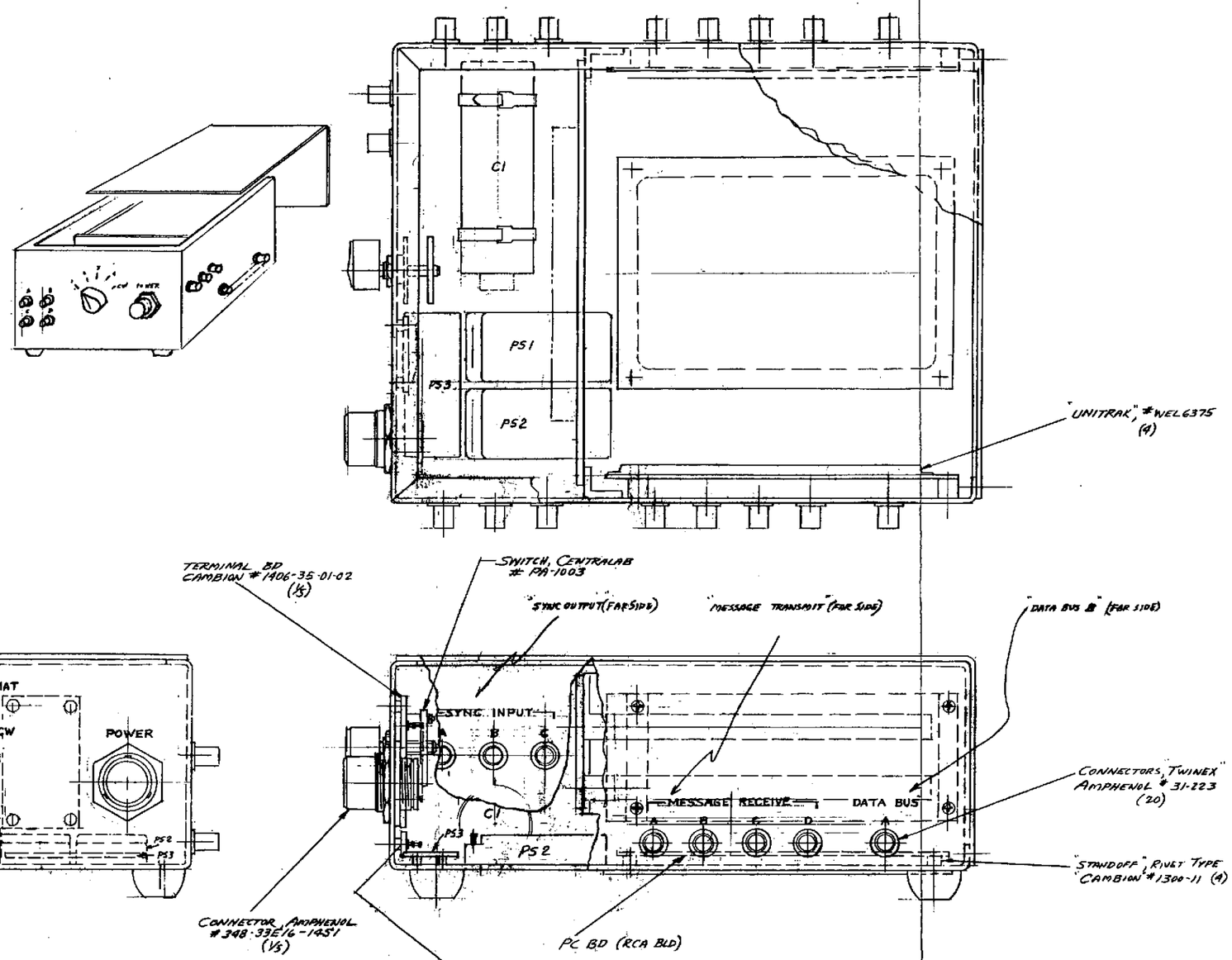
The power supply to printed board connections are provided in a cable, looped to permit disassembly for maintenance, as shown. Outline dimensions for the unit are 4-3/4 x 3 x 6-3/4.

Electronic Interface Unit

The EIU is similar in construction to the SIU. Outline dimensions and component locations are shown in Figure 22. The unit is increased in length to accommodate eleven boards (plus 2 spares).

FOLDOUT FRAME 1

FOLDOUT FRAME 2

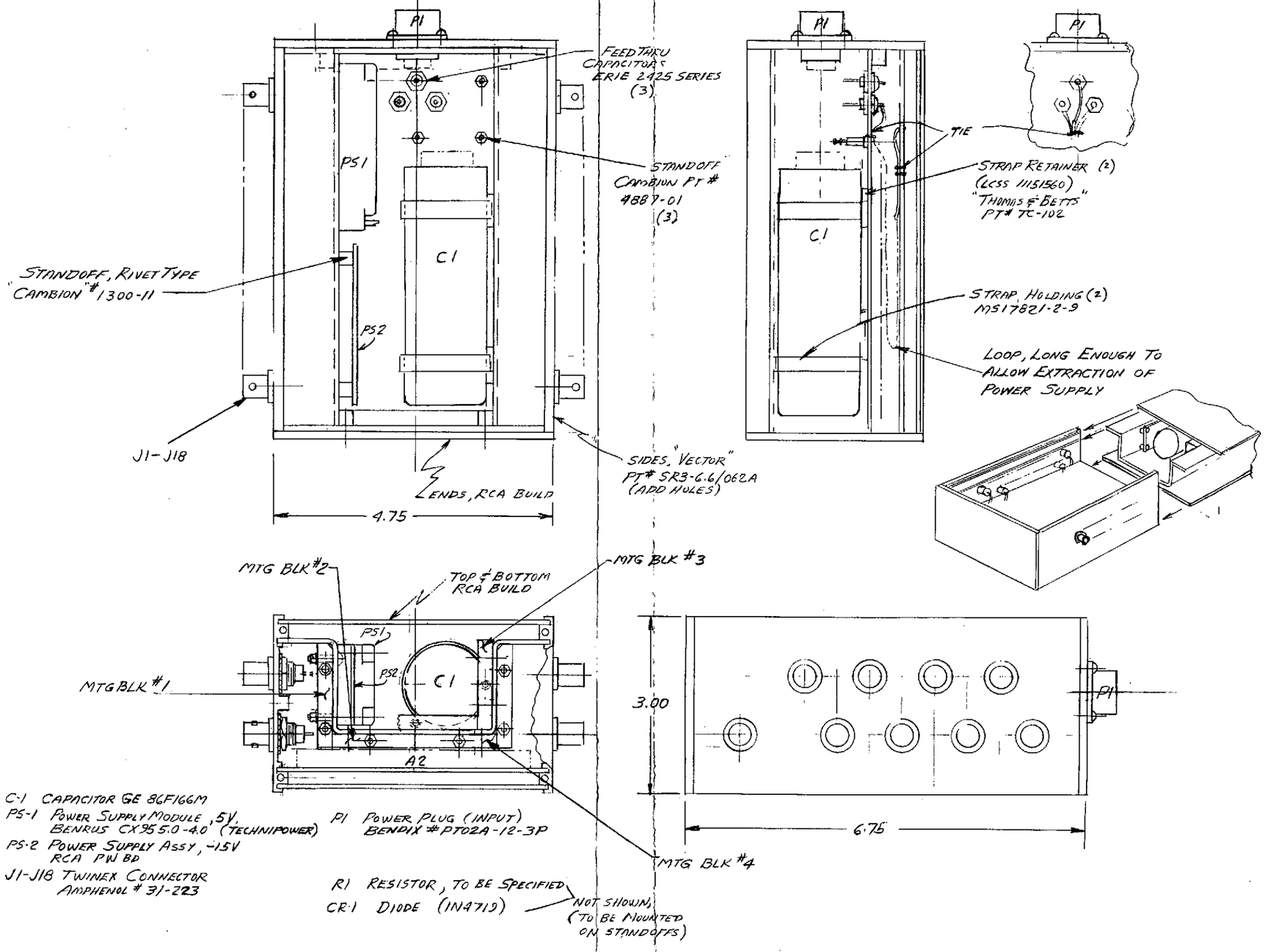


C1 CAPACITOR GE 86F166M
PS-1 POWER SUPPLY MODULE 5V CX955.0-4.0
PS-2 POWER SUPPLY MODULE 12V CX95 - - - -
PS-3 RCA BUILD (PC BD)
MISCEL SMALL PARTS MTD ON TERMINAL BDS

Figure 20. BCU Mechanical Drawing

FOLDOUT FRAME

FOLDOUT FRAME 2



C-1 CAPACITOR GE 86F166M
PS-1 POWER SUPPLY MODULE, 5V, BENRUS CX955.0-4.0 (TECHNIPOWER)
PS-2 POWER SUPPLY ASSY, -15V RCA PWB
J1-J18 TWINAX CONNECTOR AMPHENOL # 31-223

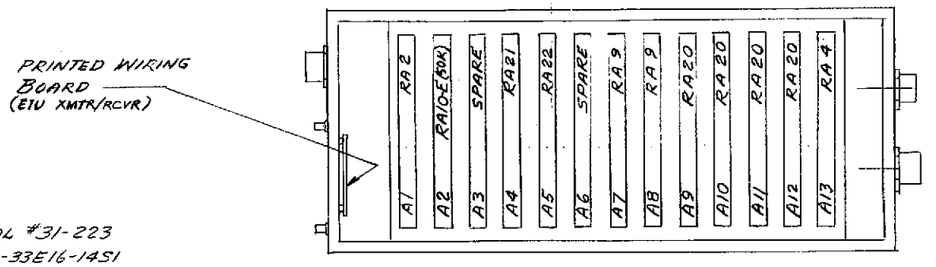
P1 POWER PLUG (INPUT) BENDIX # PT02A-12-3P

R1 RESISTOR, TO BE SPECIFIED
CR-1 DIODE (IN4719) NOT SHOWN, (TO BE MOUNTED ON STANDOFFS)

Figure 21. SIU-S Mechanical Drawing

FOLDOUT FRAME 1

FOLDOUT FRAME 2



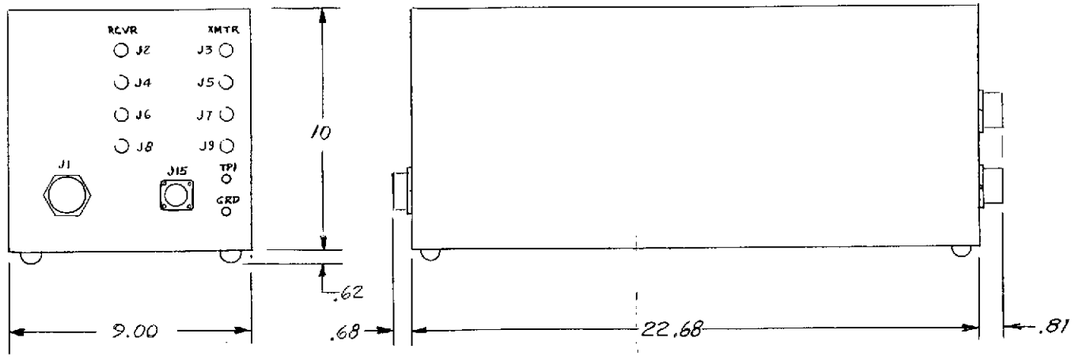
CONNECTORS:

J2 THRU J9 - AMPHENOL #31-223
J1 - AMPHENOL #348-33E16-14S1
J10 - AMPHENOL #348-33E18-8SP1
J11 THRU J14 - AMPHENOL #348-33E22-12-1S1
J15 BENDIX JTOORP12-22S005

"EIU"

CONSTRUCTION SIMILAR TO SIU & SIUP, EXCEPT LENGTHENED AS REQ'D

J.C. Hale 2-21-72



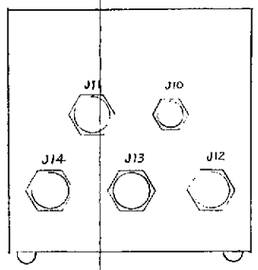


Figure 22. EIU, Board and Connector Locations

Bus Cable Set

The Bus Cable Set is similar to that provided in DBS-I.

Bus Exerciser Set

The Bus Exerciser Set is similar to that provided in DBS-I. It contains an additional plug-in board and has the front panel modified to permit operation of the four busses.

Continued Development

The basic packaging technique used was selected because it provided the maximum design flexibility, ease of modification and ease of repair consistent with an engineering model. The bulk of the components used were DIP microelectronic circuits. A plug-in mounting for these was selected permitting rapid interchangeability for troubleshooting and repair. The wirewrapped interconnections were readily modified to accommodate design changes and/or corrections.

The techniques do not, however, provide the dense packaging which will be necessary for flight hardware. The board spacing required for the wirewrapped board is 1.2 inches. Several approaches are available to increase the package density at the expense of increased costs and increased modification complexity. As flight hardware status is approached, however, the non-recurring costs will be spread over a larger number of units.

Welded Wire Interconnections

The use of welded wire board interconnections rather than wire wrap will reduce the required board spacing to 0.6 inch. The total volume reduction that can be obtained is greater than 50%. Critical features, with respect to ease of modifications are, however, retained.

Plug-in sockets for dips are provided. Modifications for welded wire assemblies, while more complex than for wire wrap assembly, are still readily accomplished. Design and production costs are comparable to wire wrap.

Multilayered Printed Boards

The use of multilayer printed boards rather than welded wire connections would reduce the total volume by 20%. Board spacing would remain at 0.6 inch, however, the volume used by the backplane assembly would be reduced. The non-recurring design costs will be higher, however, the unit costs for quantity production will be decreased and overall quality and reliability will be greater.

Hybrid Microelectronic Circuits

The most significant size reduction can be accomplished through the use of thick film hybrid microelectronic circuits. The SIU could be packaged in a 5 x 5 x 5 volume.

Since both the COS/MOS and TTL circuits are available as chips for use in the hybrid, the functions of the system are maintained. Approximately 12 to 14 chips can be provided within a typical hybrid package. The hybrids are then mounted on multilayered printed boards. Additional design costs for development of these circuits are necessary.

THE FOLLOWING PAGES ARE DUPLICATES OF ILLUSTRATIONS APPEARING ELSEWHERE IN THIS REPORT. THEY HAVE BEEN REPRODUCED HERE BY A DIFFERENT METHOD TO PROVIDE BETTER DETAIL